RE01B Group Product with 1.5-Mbyte Flash Memory

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Renesas Microcomputer

64 MHz, 32-bit Arm® Cortex®-M0+, 1.5-Mbyte flash memory supporting background operation, 256-Kbyte SRAM, energy harvesting control circuit, 2D graphic engine, 14-bit ultra-low power A/D converter, reference voltage generation circuit, RTC, sub-clock correction circuit (theoretical regulation), security function, SPI, *Bluetooth*® 5.0

Features

■ Arm® Cortex®-M0+ core
- Maximum operating frequency: 64 MHz (in boost mode)
- ARM® Memory Protection Unit (MPU)
- CoreSight™ debug port: SW-DP

■ Power-saving functions
- Back-bias control function based on silicon-on-thin-buried-oxide (SOTB™) process technology
- Operation at ultra-low power-supply voltages (from 1.62 V to 3.6 V)
- Four power control modes based on the operating frequency
- Four low power consumption modes
- Three power supply modes

■ On-chip code flash memory
- 1.5-Mbyte code flash memory
- Background programming/erasing
- No cycles of waiting for access in operation at or below 32 MHz; one cycle of waiting at frequencies above 32 MHz
- Function for area protection prevents erroneous overwriting or tampering

■ On-chip SRAM
- 256-Kbyte SRAM with no access wait cycles

■ Data transfer
- Four DMA controllers
- Single data transfer controller (DTC)

■ Reset and supply management
- Power-on reset circuit (POR)
- Low voltage detection (LVD) can be set.

■ Multiple clock sources
- External crystal oscillator (main clock): 8 to 32 MHz
- External crystal oscillator (sub-clock): 32.768 kHz
- Clock oscillator for Bluetooth: 32 MHz
- High-speed on-chip oscillator (HOCO): 24, 32, 48, or 64 MHz
- Middle-speed on-chip oscillator (MOCO): 2 MHz
- Low-speed on-chip oscillator (LOCO): 32 kHz
- Independent watchdog timer on-chip oscillator: 16 kHz
- PLL frequency synthesizer

■ Energy harvesting control
- A power generation element is directly connectable.
- High-speed startup is possible without having to wait for a secondary battery to be charged.
- Protection of a secondary battery against overcharging

■ Independent watchdog timer
- 14-bit counter, 16-kHz (1/2 LOCO clock frequency) operation

■ Sub-clock correction circuit (CCC)
- The CCC corrects the accuracy of oscillation every 16 seconds (theoretical regulation).
- Events can be generated per second in deep software standby mode.

■ Communication functions
- Single serial peripheral interface
  Single 32-bit buffer for which one command can be specified
- Single I^2C bus interface
- Two serial communications interfaces (SCIg)
  Asynchronous, clock-synchronous, simple I^2C, simple SPI, and smart card interfaces
- Single Bluetooth Low Energy module
  Includes an RF transceiver and link layer compliant with the Bluetooth 5.0 Low Energy specification
  Supports LE 1M PHY, LE 2M PHY, LE Coded PHY (125 kbps and 500 kbps), and the LE advertising extensions
  Includes a dedicated AES-CCM (128 bits) encryption circuit

PVQN0064LE-A
8 × 8 mm, 0.4-mm pitch

■ Various analog circuits
- Single 14-bit successive approximation A/D converter
  High precision: 4 channels, standard precision: 3 channels
- Single temperature sensor for measuring the internal temperature of the chip
- Reference voltage generation circuit for the 14-bit A/D converter

■ Various timer circuits
- Two general PWM timers (GPT)
  Single 32-bit counter
  Single 16-bit counter
- Two asynchronous general-purpose timers (AGT) that can be used in standby mode
- Two 8-bit timers (TMR)
- Single realtime clock (RTC)
- Single watchdog timer (WDT)
- Single low-speed timer (LST) that operates at 1 kHz
  A circuit for converting hexadecimal numbers to decimal numbers for use as a stopwatch

■ Human machine interfaces
- Single 2D graphics data conversion circuit (GDT)

■ Security functions
- Single Trusted Secure IP Lite (TSIP-Lite)
  - AES (128- or 256-bit key length, supporting ECB, CBC, CMAC, GCM, and others)
  - Key wrapping protects against the leakage of the encryption keys of users.
  - An access management circuit disables illicit access to the encryption engine.
  - Using the other security functions together with area protection enables secure booting and secure over-the-air (OTA) software updates.

■ Operating voltage and temperature range
- VCC = IOVCC = 1.62 V to 3.6 V
  IOVCCn and AVCCn can each be independently set to a voltage within the range between 1.62 V and 3.6 V.
- T_a: –40 to +85°C

1. Overview

1.1 Outline of Specifications

Table 1.1 shows the specifications in outline.

Table 1.1 Outline of Specifications (1/8)

Classification	Feature	Description
CPU	Central processing unit	• Maximum operating frequency: 64 MHz • Arm® Cortex®-M0+ - Revision: r0p1-00rel0 - Arm®v6-M architecture profile - Single-cycle integer multiplier • Arm® Memory Protection Units (MPUs) - Arm®v6 Protected Memory System Architecture - Eight protected memory areas • SysTick timer - Driven by SYSTICCLK (LOCO clock) or ICLK
Memory	Code flash memory	• Maximum 1.5 Mbytes • No cycles of waiting for access in operation at or below 32 MHz; one cycle of waiting at frequencies above 32 MHz • Prefetch function • On-board programming (three types): - Programming in serial programming mode (SCI boot mode) - Programming in on-chip debug mode - Programming by a routine for code flash memory programming within a user program
	SRAM	• Maximum 256 Kbytes SRAM0: 2000 0000h to 2000 7FFFh SRAM1: 2000 8000h to 2003 FFFFh Both areas are available during low leakage current mode. • 64 MHz, No cycles of waiting for access
Startup modes		Three startup modes: • Normal startup mode • Energy harvesting startup mode • SCI boot mode
Reset		The LSI chip supports 12 system resets and one power shutdown reset. [System resets] • RES# pin reset • Power-on reset • Independent watchdog timer reset • Watchdog timer reset • Voltage monitor 0 reset • Voltage monitor 1 reset • Voltage monitor BAT reset • Bus master MPU error reset • Bus slave MPU error reset • Stack pointer error reset • Software reset • Deep software standby reset [Power shutdown reset] • MINPWON mode reset

Table 1.1 Outline of Specifications (2/8)

Classification	Feature	Description
Low-voltage detection circuits (LVD)		The low-voltage detection circuits (LVD) monitors the voltage level input to the VCC pin or VBAT_EHC pin. The detection level can be selected using a program. • Voltage detection circuit 0 - Target for monitoring: VCC pin - Capable of generating an internal reset - The option-setting memory can be used to enable or disable the low-voltage detection circuit. - Selectable from four different voltage detection levels (1.67 V, 1.92 V, 2.17 V, and 2.42 V) • Voltage detection circuit 1 - Target for monitoring: VCC pin - The register setting can be used to enable or disable the low-voltage detection circuit. - Selectable from eight different voltage detection levels (1.67 V, 1.84 V, 2.00 V, 2.17 V, 2.33 V, 2.50 V, 2.66 V, and 2.83 V) - Digital filtering is available (1/2, 1/4, 1/8, and 1/16 LOCO frequency). - Detection of voltage rising above and falling below thresholds is selectable. - Capable of generating an internal reset - Two types of timing are selectable for release from reset. - An internal interrupt can be requested. - A maskable or non-maskable interrupt is selectable. - Voltage detection monitoring is available. - Event linking is available. • Voltage detection circuit BAT - Target for monitoring: VBAT_EHC pin - The register setting can be used to enable or disable the low-voltage detection circuit. - Selectable from five different voltage detection levels (1.67 V, 1.84 V, 2.00 V, 2.17 V, and 2.33 V) - Digital filtering is available (1/2, 1/4, 1/8, and 1/16 LOCO frequency). - Detection of voltage rising above and falling below thresholds is selectable. - Capable of generating an internal reset - Two types of timing are selectable for release from reset. - An internal interrupt can be requested. - A maskable or non-maskable interrupt is selectable. - Voltage detection monitoring is available.
Clock		• The LSI chip has the following clock generation circuits. - Main clock oscillator (MOSC) - Sub-clock oscillator (SOSC) - High-speed on-chip oscillator (HOCO) - Middle-speed on-chip oscillator (MOCO) - Low-speed on-chip oscillator (LOCO) - PLL frequency synthesizer - IWDT-dedicated on-chip oscillator (IWDTLOCO) - Bluetooth-dedicated clock oscillator - Bluetooth-dedicated low-speed on-chip oscillator • Clock output support - CLKOUT32K pin (capable of the output of the SOSC clock signal)

Table 1.1 Outline of Specifications (3/8)

Classification	Feature	Description
Clock frequency accuracy measurement circuit (CAC)		The CAC checks the system clock frequency with a reference clock signal by counting the number of pulses of the system clock to be measured. Event signals can be generated when the frequency does not match or measurement ends. This function is particularly useful in implementing a fail-safe mechanism for home and industrial automation applications. • Target clocks for measurement - Main clock - Sub-clock - HOCO clock - MOCO clock - LOCO clock - CCC2K clock - IWDT-dedicated clock - Peripheral module clock B (PCLKB) • Reference clocks for measurement - Main clock - Sub-clock - HOCO clock - MOCO clock - LOCO clock - CCC2K clock - IWDT-dedicated clock - Peripheral module clock B (PCLKB) • Digital filtering is selectable.
Low power consumption	Power-saving functions	The LSI chip has several functions for power saving, such as setting clock dividers, stopping modules, selecting power control mode in operating mode, transitioning to low power consumption mode, and power supply mode per domain. • Three power control modes based on the operating frequency - Boost mode (up to 64 MHz) - Normal mode - High-speed mode (up to 32 MHz) - Low-speed mode (up to 2 MHz) - Subosc-speed mode (this LSI chip can be placed in the low leakage current mode at 32.768 kHz.) - Low leakage current mode (32.768 kHz) • Five low-power consumption modes - Operating mode - Sleep mode - Software standby mode - Snooze mode - Deep software standby mode • Three power supply modes - All-power supply mode (ALLPWON) - Flash-excluded power supply mode (EXFPWON) - Minimum power supply mode (MINPWON)
	Back-bias voltage control*1 (VBBC) function	Program control of the back bias voltage enables low leakage current operation in the low leakage current mode.
Energy harvesting control circuit (EHC)		Starting up of this LSI chip in the power-saving mode is possible by controlling the power generating element, storage capacitor, and secondary battery.
Register write protection (RWP)		The register write protection function protects important registers from rewrites caused by software errors.
Memory protection units (MPUs) and stack pointer monitors		• Illicit memory access - CPU (attempt at access to an undefined address space) - CPU stack pointer monitors: Two regions • Memory protection - Arm® MPU: Eight areas - Bus master MPU: Four areas - Bus slave MPU • Security - Security MPU: Two secure program areas Three secure data areas (code flash memory, SRAM, and TSIP-Lite)

Table 1.1 Outline of Specifications (4/8)

Classification	Feature	Description
Interrupt	Interrupt controller unit (ICU)	• Peripheral function interrupts: 103 sources • External interrupts: Five sources (IRQ0, IRQ1, and IRQ5 to IRQ7) • Non-maskable interrupts: Eight sources • DMAC and DTC control: The DMAC and DTC can be activated by interrupt sources. • Interrupts for NVIC: 29 sources
Key interrupt function (KINT)		An interrupt can be generated by inputting a rising or falling edge to the key interrupt input pins.
DMA	Data transfer controller (DTC)	• Transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: External interrupts and interrupt requests from peripheral functions • Transfer channels: Multiple data units can be transferred on a single activation source (chain transfer).
	DMA controller (DMAC)	A 4-channel DMA controller (DMAC) module is incorporated for transferring data without CPU intervention. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. • Transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
Event link controller (ELC)		The ELC uses the interrupt requests generated by various peripheral modules as event signals and connects them to different modules. This enables modules to function in combination with each other without CPU intervention.
Timers	General PWM timer (GPT)	• Single 32-bit counter (GPT32), and single 16-bit counter (GPT16) • Up-counting or down-counting (saw waves) or up-counting or down-counting (triangle waves) is selectable for each counter. • Two input/output pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four buffer registers are provided and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms. • Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow) • Generation of dead times in PWM operation • Synchronous starting, stopping and clearing counters for arbitrary channels • Based on the ELC settings, up to four ELC events can start or stop counting, clear the counter, drive counting up or down, or trigger input capture. • The states of two input pins can be detected to start or stop counting, clear the counter, drive counting up or down, or trigger input capture. • Up to two external triggers can start or stop counting, clear the counter, drive counting up or down, or trigger input capture. • Output pin disable function in response to detecting short-circuits between output pins • Compare match A to D events, and overflow or underflow events can be output to the ELC. • A noise filter can be used for input capture input.
	Port output enable for GPT (POE)	• Output disabling in response to detection of the input level on the GTETRGn pin • Output disabling in response to a request from the GPT. • Output disabling in response to detection of stopped oscillation. • Output disabling in response to software register settings. • The GTETRGn signals can be output to the GPT as external trigger signals after polarity and filter selection. • An input filter can be used for the GTETRGn pin.

Table 1.1 Outline of Specifications (5/8)

Classification	Feature	Description
Timers	Asynchronous general-purpose timer (AGT)	The asynchronous general-purpose timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. • Two channels • Timer mode • The AGT supports the interrupt and event link functions for three sources, and the chip can return from software standby mode. - Underflow event signal/measurement complete event signal - Compare match A event signal - Compare match B event signal
	8-bit timers (TMR)	• (8 bits × 2 channels) × 1 unit • Select from among seven internal clock signals (PCLKB/1, PCLKB/2, PCLKB/8, PCLKB/32, PCLKB/64, PCLKB/1024, PCLKB/8192) and one external clock signal. • Capable of output of pulse with desired duty cycles or of PWM signals • The two channels can be cascaded to create a 16-bit timer. • Conversion start trigger for the 14-bit A/D converter can be generated. • Support of function for event linking by the ELC
	Realtime clock (RTC)	The RTC has two counting modes: a calendar count mode and a binary count mode. These modes are controlled by the register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (western) calendar. • Clock source: Sub-clock oscillator • Counting by either clock counters or 32-bit binary counters in second units is selectable. • Clock and calendar functions • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Time capture function • Support of function for event linking by the ELC
	Clock correction circuit (CCC)	The CCC corrects the oscillation accuracy every 16 seconds for the sub-clock (32.768 kHz). • Clock output after correction: 2.048 kHz or 512 Hz • Signal output (CCCOUT): Selectable from 512 Hz, 1 Hz, and RTC output (1 Hz or 64 Hz) • Support of function for event linking by the ELC
	Watchdog timer (WDT)	The WDT can be used to reset the LSI chip when the system runs out of control. A non-maskable interrupt or interrupt can be generated by an underflow of the counter. • 14 bits × 1 channel • Count clock (WDTCLK): Selectable from PCLKB and CCC_2K • Selectable counter clock signal: 6 types (WDTCLK/4, WDTCLK/64, WDTCLK/128, WDTCLK/512, WDTCLK/2048, WDTCLK/8192).
	Independent watchdog timer (IWDT)	The IWDT is a 14-bit down-counter and operates with the clock (IWDTCLK) that is independent of the clock used by the system. It can reset the LSI chip if the system runs out of control. The IWDT provides functionality to reset the LSI chip or to generate a non-maskable interrupt or interrupt on a counter underflow. • 14 bits × 1 channel • Counter-input clock: IWDTLOCO • IWDTLOCO/1, IWDTLOCO/16, IWDTLOCO/32, IWDTLOCO/64, IWDTLOCO/128, IWDTLOCO/256 • Window function: The positions where the window starts and ends are specifiable (the window defines the timing with which refreshing is enabled and disabled). • Support of function for event linking by the ELC
	Low-speed clock timer (LST)	The low-speed clock timer (LST) is a 13-bit timer that consists of a 1-kHz timer-counter and a circuit for converting hexadecimal numbers to decimal numbers. The LST can be used to indicate a count that needs to be displayed in decimal. • Capable of counting from 0.000 to 1.999 seconds (in units of 0.001 seconds) • The counted value can be directly stored in a register in decimal notation.

Table 1.1 Outline of Specifications (6/8)

Classification	Feature	Description
Communications interfaces	Serial communications interfaces (SCIg)	Without FIFO (SCIg) × 2 channels The SCI is configurable for five asynchronous and synchronous serial interfaces. • Asynchronous interfaces (UART and asynchronous communications interface adapter (ACIA)) • 8-bit clock-synchronous interface • Simple I²C (master-only) • Simple SPI • Smart card interface The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. The data transfer speed can be configured independently using an on-chip baud rate generator. • Selectable as LSB-first or MSB-first transfer • Support of function for event linking by the ELC (SCI2 only)
	I²C bus interface (RIIC)	The RIIC conforms with and provides a subset of the NXP I²C bus (Inter-Integrated Circuit bus) interface functions. • I²C bus format or SMBus format • Master or slave selectable • Automatic securing of the setup times, hold times, and bus-free times for the multi-master transfer rate • Support of function for event linking by the ELC
	Serial peripheral interface (SPI)	The SPI can handle high-speed and full-duplex synchronous serial communications with multiple processors and peripheral devices. • One command/32-bit buffer × 1 channel • Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals allows serial communications through SPI operation (four-wire method) or clock synchronous operation (three-wire method). • Transmit-only operation is available. • Switching of RSPCK polarity • Switching of RSPCK phase • MSB-first or LSB-first selectable • Transfer bit length selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits • 32-bit transmit and receive buffers • Up to one frame can be transferred in one round of transmission or reception (a frame consisting of up to 32 bits). • Double buffer configuration for the transmission and reception buffers
	Bluetooth Low Energy (BLE)	• Includes an RF transceiver and link layer compliant with the Bluetooth 5.0 Low Energy specification • Supports LE 1M PHY, LE 2M PHY, LE Coded PHY (125 kbps and 500 kbps), and the LE advertising extensions • Includes a dedicated AES-CCM (128 bits) encryption circuit

Table 1.1 Outline of Specifications (7/8)

Classification	Feature	Description
Analog	14-bit A/D converter (S14AD)	A 14-bit successive approximation A/D converter incorporated Up to seven analog input channels are selectable. The analog input channels and the temperature sensor output are selectable for conversion. The A/D conversion accuracy is selectable between 12-bit and 14-bit conversion making it possible to optimize the tradeoff between speed and resolution in generating a digital value. • 14 bits × up to seven channels (four for high accuracy and three for standard) • Resolution: 14 bits (14-bit or 12-bit conversion selectable) • Operating mode: Scan mode (single-scan mode, continuous-scan mode, or group-scan mode) • Group A priority control (only for group-scan mode) • Variable sampling state count • A/D-converted value addition mode or average mode selectable • Disconnection detection assist function • Double-trigger mode (duplication of A/D conversion data) • Support of function for event linking by the ELC • Automatic clear function of A/D data registers • Compare function for window A and window B • Digital compare function Comparison of values in the comparison register and the data register, and comparison between values in the data registers
	Temperature sensor (TEMPS)	The temperature sensor outputs the voltage that is directly proportional to the die temperature. The output voltage is converted to a digital value by the S14AD for conversion and can be further used by the end application.
	Reference voltage generation circuit (VREF)	The circuit generates two types (1.25 V/2.5 V) of reference voltage. The generated voltage can be used as the reference voltage for the ADC.
Human machine interfaces (HMI)	2D graphics data conversion circuit (GDT)	A graphic accelerator circuit that handles 2D image processing incorporated • Handling of up to 32-byte image data. Up to 63 × 64 bits for conversion of glyph data into image data. • Rotations of 90-degree clockwise, 90-degree counterclockwise, vertical flip, and horizontal flip • Scaling down to 1/8, 2/8, 3/8, 4/8, 5/8, 6/8, or 7/8 by pixel averaging and to 1/2 by pixel skipping • Inversion allows bit-wise inversion of images; 1 is inverted to 0, and vice versa. • Monochrome compositing of a foreground image, background image, and trimming image • Color compositing of a foreground image and background image, and setting of priority color and transparent color • Scrolling of an image in 1-bit units • Conversion of glyph data into image data • Colorization of monochrome images by RGB values • Color data sorting allows separate R, G, and B images in memory to be sorted into a single area in order of R, G, and B. • Endian conversion
Data processing	Cyclic redundancy check (CRC) calculator	The CRC calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communications. Additionally, various CRC generation polynomials are available. • CRC code generated for any data in 8-bit/32-bit units • 8-bit data: One of three polynomials selectable [8-bit CRC] $X^8 + X^2 + X + 1$ (CRC-8) [16-bit CRC] $X^{16} + X^{15} + X^2 + 1$ (CRC-16) $X^{16} + X^{12} + X^5 + 1$ (CRC-16-CCITT) • 32-bit data: One of two polynomials selectable [32-bit CRC] $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (CRC-32) $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ (CRC-32C) • The bit order of CRC calculation results can be switched for LSB- or MSB-first communications.

Table 1.1 Outline of Specifications (8/8)

Classification	Feature	Description
Data processing	Data operation circuit (DOC)	The DOC compares, adds, and subtracts 16-bit data.
	Divider (DIV)	A circuit for handling high-speed division for signed 32-bit fixed point data • Dividend: Signed 32-bit data • Divisor: Signed 32-bit data
	Data inversion circuit (DIL)	A circuit for inverting the values of input data is integrated.
Security	Trusted secure IP lite (TSIP-Lite)	• Access management circuit available • Security algorithms: - Common key cryptosystem (symmetrical cryptography): AES key length: 128 bits/ 256 bits - Encryption usage modes: GCM, ECB, CBC, CMAC, XTS, CTR, GCTR, CCM • Other support features: - TRNG (true random number generation circuit) - Hash value generation: GHASH - Support for unique IDs (128-bit unique IDs)
Operating frequency		Up to 32 MHz (normal mode) Up to 64 MHz (boost mode) Up to 32 kHz (low leakage current mode)
Power supply voltages		VCC = IOVCC = 1.62 to 3.6 V, IOVCC0 = 1.62 to 3.6 V, IOVCC1 = 1.62 to 3.6 V, IOVCC2 = 1.62 to 3.6 V, IOVCC3 = 1.62 to 3.6 V, AVCC0 = 1.62 to 3.6 V, VCC_RF = 1.8 to 3.6 V, AVCC_RF = 1.8 to 3.6 V, 1.62 V ≤ VREFH0 ≤ AVCC0
Operating ambient temperature		–40 to +85°C
Package		64-pin QFN (PVQN0064LE-A)
On-chip debugging system		• Debug and trace: DWT, BPU, CoreSight™ MTB-M0+ • CoreSight debug port: SW-DP

Note 1. Voltage for charging the VBP and VBN pins

1.2 Block Diagram

Figure 1.1 is a block diagram of this chip.

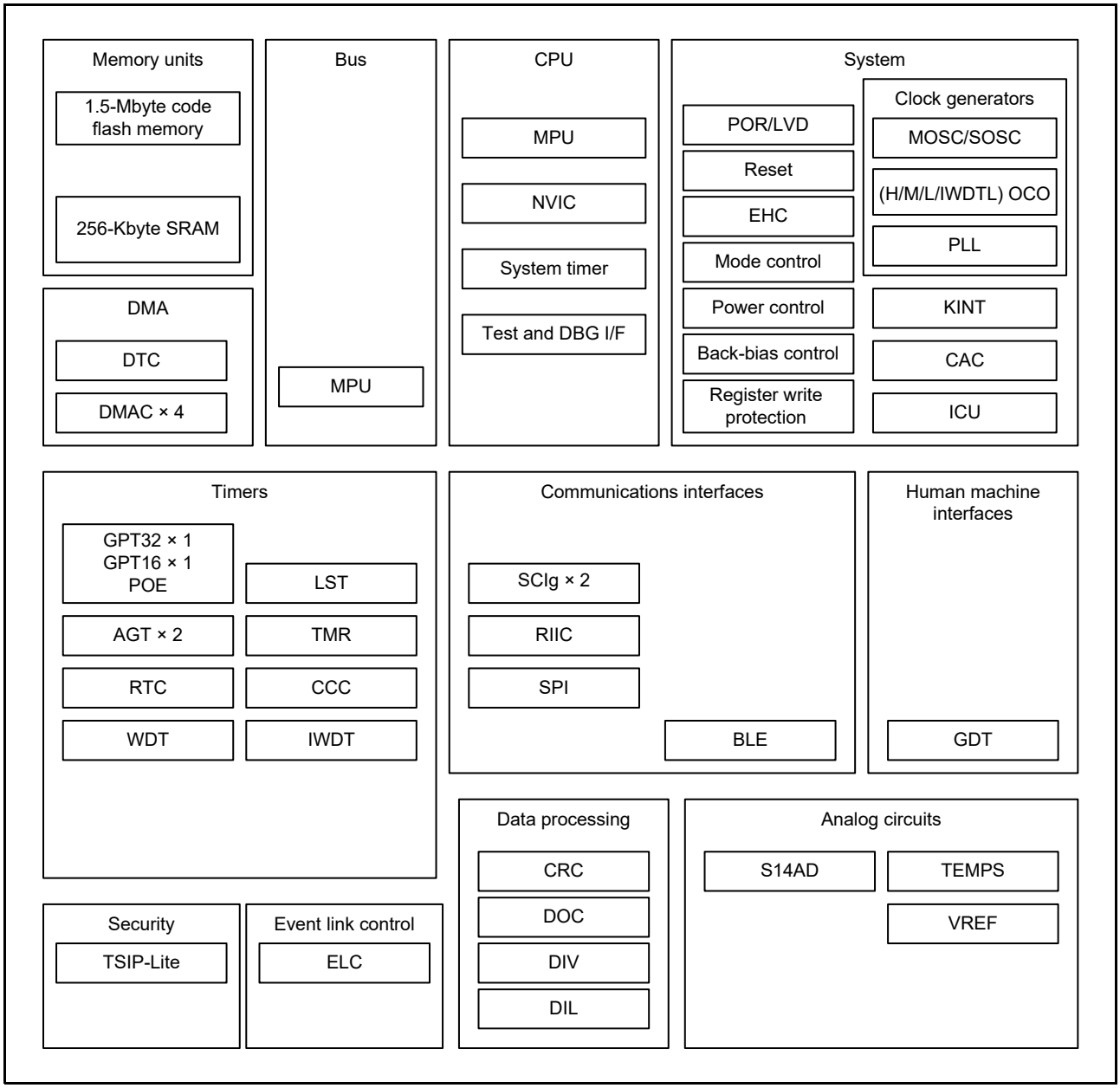


Figure 1.1 Block Diagram

1.3 List of Products

Table 1.2 List of Products

Part Number	Package	Code Flash Memory Capacity	SRAM Capacity	Support Status
				TSIP-Lite
R7F0E01BD2DNB	PVQN0064LE-A	1.5 Mbytes	256 Kbytes	Supported

1.4 Function Comparison

Table 1.3 lists the functions of this product.

Table 1.3 List of Functions

Part Number			R7F0E01BD2DNB
Total pin count			64
Number of general-purpose I/O port pins	I/O port pins		27
	Input port pin		1
Package			QFN
Code flash memory			1.5 Mbytes
SRAM			256 Kbytes
CPU operating frequency			32 MHz (normal mode) 64 MHz (boost mode) 32 kHz (low leakage current mode)
Interrupt control		ICU	Yes
		IRQ	Channels 0, 1, and 5 to 7
Key interrupt		KINT	2 channels
DMA		DTC	Yes
		DMAC	Channels 0 to 3
Event control		ELC	Yes
Energy harvesting		EHC	Yes
Back-bias voltage control		VBBC	Yes
Timers	GPT32		Channel 0
	GPT16		Channel 3
		POE	Yes
	AGT		Channels 0 and 1
	TMR		Channels 0 and 1
	RTC		Yes
	CCC		Yes
	WDT		Yes
	IWDT		Yes
	LST		Yes
Communications function	SCIg	w/o FIFO	Channels 2 and 3
	RIIC		Channel 1
	SPI	32-bit buffer	Channel 1
	Bluetooth Low Energy		Yes
Analog	S14AD	High precision	4 channels
		Standard precision	3 channels
	TEMPS		Yes (1 channel)
	VREF		Yes (1 channel)
HMI graphics	GDT		Yes
Data processing	CRC		Yes
	DOC		Yes
	DIV		Yes
	DIL		Yes
Security	TSIP-Lite		Yes

1.5 Pin Functions

Table 1.4 lists the pin functions. For details on how to connect smoothing capacitors, refer to examples of their connection shown and described in Appendix B.

Table 1.4 Pin Functions (1/4)

Function	Pin Name		I/O	Description
Power supply	VCC/ IOVCC	Normal startup mode	Input	Power supply pin. Connect it to the system power supply. Connect to VSS through a 0.1-µF smoothing capacitor. Place the smoothing capacitor close to the pin.*2 Apply the voltage to this pin before the voltage for the IOVCCn pin.
		Energy harvesting startup mode	Input	Power supply pin. Connect it to the system power supply. Connect to VSS through 0.1-µF smoothing capacitor (1). Place the smoothing capacitor close to the pin. In addition, connect to VSS through smoothing capacitor (2) having capacity of 1/10 of capacity of a storage capacitor connected to the VCC_SU pin to improve robustness against external noise and obtain stable operation of the circuit. For instance, connect a 4.7-µF smoothing capacitor in the case where a 47-µF storage capacitor is connected to the VCC_SU pin. If placing the smoothing capacitor (2) close to this pin is possible, the smoothing capacitor (1) is not required. For more details, see Appendix B. Connecting the Capacitors to the Power Supply Pins.
	VSS		Input	Ground pin. Connect it to the system power supply (0 V).
	VCL		Input	Internal power supply stabilization pin. Connect the pin to VSS through a 4.7-µF smoothing capacitor. Place the smoothing capacitor close to the pin.
	VCLH		Input	Internal power supply stabilization pin. Separately from the VCL pin, connect the VCLH pin to VSS through a 4.7-µF smoothing capacitor. Place the smoothing capacitor close to the pin.
	VBN		—	Back-bias voltage stabilization pins. Connect the respective pins to VSS through a 1.0-µF smoothing capacitor. Place the smoothing capacitor close to the pin.
	VBP		—	
	VSC_VCC	Normal startup mode	Input	Power supply pin supplied from a power generation element. Connect it to the system power supply (0 V) in normal startup mode.
		Energy harvesting startup mode	Input	Power supply pin supplied from a power generation element. Connect this pin to VSC_GND through a smoothing capacitor in parallel with the power generation element. Place the smoothing capacitor close to the pin. While a smoothing capacitor with a capacitance value of 4.7-nF to 47-nF is recommended, select a capacity value suitably in accordance with stability of a power generating element or the like.
	VCC_SU	Normal startup mode	I/O	Power supply pin supplied from a storage capacitor. Short it to VCC/ IOVCC in normal startup mode.
		Energy harvesting startup mode	I/O	Power supply pin supplied from a storage capacitor. When using a photovoltaic cell as a power generating element, connect a storage capacitor with a capacitance value in accordance with an operating temperature, and with a value of at least 10 times VCC. A capacitance value of 47 µF is required at 25°C. As a temperature becomes higher, a larger capacitance value is required. See the EHC characteristics in section 6.9, EHC Characteristics. Connect this pin to a 100-µF storage capacitor in the case where other power generating elements are used.
	VSC_GND		Input	VSC_VCC ground pin. Connect it to the system power supply (0 V).
	VBAT_EHC	Normal startup mode	Input	Power supply pin supplied from a secondary battery. Connect it to VCC/IOVCC in normal startup mode.
		Energy harvesting startup mode	Input	Power supply pin supplied from a secondary battery. Connect a 2.6-V or 3.0-V secondary battery or a super capacitor in energy harvesting startup mode.

Table 1.4 Pin Functions (2/4)

Function	Pin Name	I/O	Description
Power supply	IOVCCn (n = 0 to 3)	Input	Power supply pin for input/output. Connect the pin to VSS through a 0.1-µF smoothing capacitor. Place the smoothing capacitor close to the pin.*2, *3 This pin can be left open-circuit when not in use. When the pin is to be used, set the corresponding bit in the power supply open control register (VOCR) described in section 12.2.23 in the User's Manual: Hardware.
Clock	XTAL	Input	Pins for connecting the MOSC resonator EXTAL is an external clock input pin.
	EXTAL	Output	
	XCIN	Input	Pins for connecting the SOSC resonator
	XCOUT	Output	
	XTAL1_RF	Input	Pins for connecting the Bluetooth-dedicated clock oscillator. Connect a 32-MHz oscillator to these pins.
	XTAL2_RF	Output	
	CLKOUT32K	Output	SOSC clock output pin
Startup mode control	MD	Input	Pin for setting the startup mode. The signal level on this pin must not be changed during transition to the specified startup mode after release from the reset state.
	EHMD	Input	Pin for setting the energy harvesting mode
System control	RES#	Input	Reset signal input pin. The LSI chip enters the reset state when this signal goes low.
Interrupts	NMI	Input	Non-maskable interrupt request pin
	IRQ0, IRQ1, IRQ5 to IRQ7, IRQ0_A_DS, IRQ1_A_DS	Input	Maskable interrupt request pins Pins that have"_DS" appended to their names can be used as triggers for release from deep software standby.
KINT	KRM02, KRM07	Input	A key interrupt can be generated by inputting a falling edge to the key interrupt input pins.
On-chip debugger	SWDIO	I/O	SWD data input/output pin
	SWCLK	Input	SWD clock input pin
GPT, POE	GTIOC0A, GTIOC3A, GTIOC0B, GTIOC3B	I/O	Input capture, output compare, or PWM output pins
	GTETRGA, GTETRGB	Input	External trigger input pins
AGT	AGTOB1	Output	Compare match B output pin
TMR	TMCI0, TMCI1	Input	Input pins for external clocks to be input to the counter
	TMRI0, TMRI1	Input	Input pins for the counter reset
	TMO0, TMO1	Output	Compare match output pins
RTC	RTCIC2	Input	Time capture event input pin
	RTCOUT	Output	Output pin for 1-Hz or 64-Hz clock
CCC	CCCOUT	Output	CCC clock output pin
SCIg	[Asynchronous mode/clock synchronous mode]		
	SCK2, SCK3	I/O	Input/output pins for the clock (clock synchronous mode)
	RXD2, RXD3	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXD2, TXD3	Output	Output pins for transmit data (asynchronous mode/clock synchronous mode)
	CTS2, CTS3	Input	Input pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode)
	RTS2, RTS3	Output	Output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode)
	[Simple I²C mode]		
	SSCL2, SSCL3	I/O	Input/output pins for the I²C clock (simple I²C mode)
	SSDA2, SSDA3	I/O	Input/output pins for the I²C data (simple I²C mode)

Table 1.4 Pin Functions (3/4)

Function	Pin Name	I/O	Description
SCIg	[Simple SPI mode]		
	SCK2, SCK3	I/O	Input/output pins for the clock (simple SPI mode)
	MISO2, MISO3	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSI2, MOSI3	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SS2, SS3	Input	Chip-select input pins (simple SPI mode)
RIIC	SCL1	I/O	Input/output pin for clock
	SDA1	I/O	Input/output pin for data
SPI	RSPCKB	I/O	Clock input/output pin
	MOSIB	I/O	Input/output pin for data output from the master
	MISOB	I/O	Input/output pin for data output from the slave
	SSLB2, SSLB3	Output	Output pins for slave selection
Analog power supply	AVCC0	Input	Analog power supply pin for the 14-bit A/D converter, reference voltage generation circuit, and temperature sensor. Connect the pin to AVSS0 through a 1.0-µF smoothing capacitor. Place the smoothing capacitor close to the pin.*4 This pin can be left open-circuit when not in use. When the pin is to be used, set the corresponding bit in the power supply open control register (VOCR) described in section 12.2.23 in the User's Manual: Hardware.
	AVSS0	Input	Analog ground pin for the 14-bit A/D converter, reference voltage generation circuit, and temperature sensor. This pin can be left open-circuit when not in use. When the pin is to be used, set the corresponding bit in the power supply open control register (VOCR) described in section 12.2.23 in the User's Manual: Hardware.
	VREFH0	Input	Analog reference voltage pin for the 14-bit A/D converter. Connect the pin to VREFL0 through a 1.0-µF smoothing capacitor. Place the smoothing capacitor close to the pin.*5 Connect this pin to AVCC0 when not using the A/D converter. Leave this pin open-circuit if AVCC0 is not to be supplied.
	AVTRO	Output	When using the output from the reference voltage generation circuit (VREF) as the reference voltage, connect this to VREFL0 through a 10-µF smoothing capacitor.
	VREFL0	Input	Analog reference ground pin for the 14-bit A/D converter. Connect this pin to AVSS0 when not using the A/D converter. Leave this pin open-circuit if AVCC0 is not to be supplied.
S14AD	AN000 to AN003, AN022, AN027, AN028	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0	Input	Input pin for the external trigger signal that starts A/D conversion
BLE	ANT	I/O	RF single input and output pin for the RF transceiver Set the impedance of the signal line to 50 Ω.
	DCLOUT	Output	RF transceiver power-supply output pin
	DCLIN_A	Input	RF transceiver power-supply output connection pin
	DCLIN_D	Input	RF transceiver power-supply output connection pin
	VCC_RF	Input	RF transceiver power-supply pin
	AVCC_RF	Input	RF transceiver power-supply pin
	VSS_RF	Input	RF transceiver ground pin

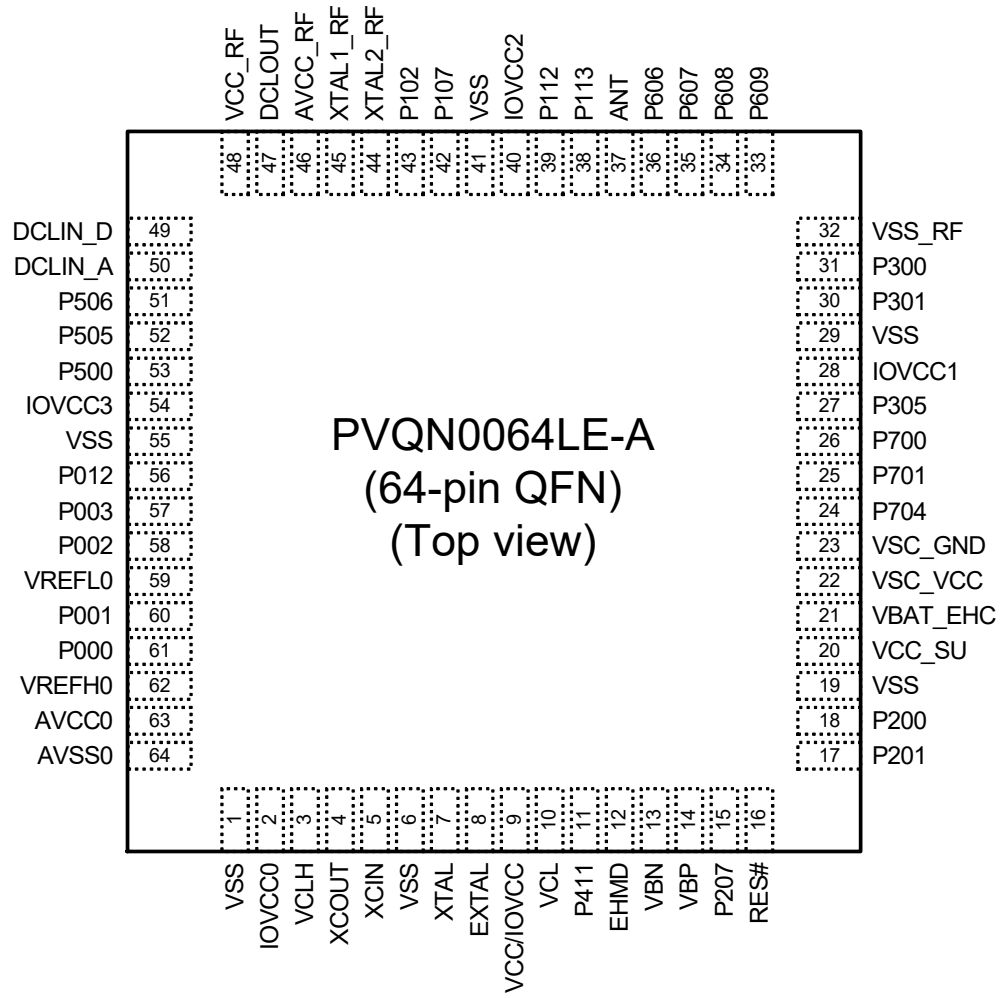
Table 1.4 Pin Functions (4/4)

Function	Pin Name	I/O	Description
I/O ports	P000 to P003, P012	I/O	5-bit input/output pins
	P102, P107, P112, P113	I/O	4-bit input/output pins
	P200	Input	1-bit input-only pin. Multiplexed with the NMI pin function.
	P201, P207	I/O	2-bit input/output pins
	P300, P301, P305	I/O	3-bit input/output pins
	P411	I/O	1-bit input/output pin
	P412, P413	I/O	2-bit input/output pins. Multiplexed with the EXTAL and XTAL pin functions.
	P500, P505, P506	I/O	3-bit input/output pins
	P606 to P609	I/O	4-bit input/output pins
	P700, P701, P704	I/O	3-bit input/output pins

Note: Use a laminated ceramic capacitor as a smoothing capacitor.
Note 1. For the SCIg interfaces, each communications pin has multiple functions that work differently depending on the mode as follows: RXDn/SCLn/MISOn, TXDn/SDAn/MOSIn, CTSn/RTSn/SSn
Note 2. In an environment where there is much external noise, optionally connect these pins to VSS through a 10-pF smoothing capacitor close to the respective current sources to improve robustness against external noise and obtain stable operation of the circuit.
Note 3. When some of the IOVCC0, IOVCC1, IOVCC2, and IOVCC3 pins are connected at the same voltage, a 10-µF smoothing capacitor can be shared. In the case where the pin is connected to VCC/IOVCC, a 10-µF smoothing capacitor is not necessary.
Note 4. In an environment where there is much external noise, optionally connect this pin to AVSS0 through a 10-pF smoothing capacitor close to the current source to improve robustness against external noise and obtain stable operation of the circuit.
Note 5. In an environment where there is much external noise, optionally connect this pin to VREFL0 through a 10-pF smoothing capacitor close to the current source to improve robustness against external noise and obtain stable operation of the circuit.

1.6 Pin Arrangement

Figure 1.2 shows pin arrangement.



Note: The pin arrangement diagram indicates the positions of power supply pins and I/O ports.
For the full pin configuration, see Table 1.5, List of the Pins and Multiplexed Pin Functions (64-Pin QFN).

Figure 1.2 Pin Arrangement for 64-Pin QFN

1.7 List of Pins

Table 1.5 is list of the pins and multiplexed pin functions.

Table 1.5 List of the Pins and Multiplexed Pin Functions (64-Pin QFN) (1/2)

Pin Number 64QFN	Power Supply, Clock, System Control	I/O Port	Timers (CAC, GPT, POE, AGT, TMR, RTC)	Communications (SCI, SPI, RIIC)	Interrupts (IRQ, KINT)	Analog (S14AD)	Applicable Power Supply	Communi-cations (BLE)
1	VSS							
2	IOVCC0							
3	VCLH							
4	XCOUT						IOVCC	
5	XCIN						IOVCC	
6	VSS							
7	XTAL	P413	GTETRGA_A/GTIOC0A_A	TXD3_A/SSDA3_A/ MOSI3_A			IOVCC	
8	EXTAL	P412	GTETRGB_A/GTIOC0B_A	RXD3_A/SSCL3_A/ MISO3_A			IOVCC	
9	VCC/IOVCC							
10	VCL							
11	CLKOUT32K_ A/SWCLK	P411	TMCI0_A	SCK3_A/TXDSP	IRQ0_A_DS		IOVCC	
12	EHMD						IOVCC	
13	VBN							
14	VBP							
15	SWDIO	P207		CTS3_A/RTS3_A/ SS3_A/RXDSP	IRQ1_A_DS		IOVCC	
16	RES#						IOVCC	
17	MD	P201	TMRI0_A				IOVCC	
18		P200	TMO0_A		NMI		IOVCC	
19	VSS							
20	VCC_SU							
21	VBAT_EHC							
22	VSC_VCC							
23	VSC_GND							
24		P704	TMCI1				IOVCC1	
25		P701	TMRI1/RTCIC2_B	SCL1			IOVCC1	
26		P700	TMO1	SDA1			IOVCC1	
27		P305					IOVCC1	
28	IOVCC1							
29	VSS							
30		P301	TMRI0_B/CCCOUT_A/ RTCOUT_A				IOVCC1	
31		P300	TMO0_B				IOVCC1	
32								VSS_RF
33		P609		TXD2_C/SSDA2_C/ MOSI2_C/MOSIB_B			IOVCC1	
34		P608	GTETRGA_C	RXD2_C/SSCL2_C/ MISO2_C/MISOB_B			IOVCC1	
35		P607	GTETRGB_C	CTS2_C/RTS2_C/ SS2_C/RSPCKB_B			IOVCC1	
36		P606		SCK2_C/SSLB2_B			IOVCC1	
37								ANT
38		P113	GTIOC3A_A	SSLB2_A	IRQ5_A		IOVCC2	
39		P112	GTIOC3B_A	SSLB3_A	IRQ6_A		IOVCC2	

Table 1.5 List of the Pins and Multiplexed Pin Functions (64-Pin QFN) (2/2)

Pin Number 64QFN	Power Supply, Clock, System Control	I/O Port	Timers (CAC, GPT, POE, AGT, TMR, RTC)	Communications (SCI, SPI, RIIC)	Interrupts (IRQ, KINT)	Analog (S14AD)	Applicable Power Supply	Communi-cations (BLE)
40	IOVCC2							
41	VSS							
42		P107	AGTOB1_A		IRQ7_A/ KRM07_A		IOVCC2	
43		P102		TXD2_A/SSDA2_A/ MOSI2_A	KRM02_A		IOVCC2	
44								XTAL2_RF
45								XTAL1_RF
46								AVCC_RF
47								DCLOUT
48								VCC_RF
49								DCLIN_D
50								DCLIN_A
51		P506			IRQ0_C	AN028	IOVCC3	
52		P505			IRQ1_C	AN027	IOVCC3	
53		P500	ADTRG0_B/AGTOB1_B			AN022	IOVCC3	
54	IOVCC3							
55	VSS							
56		P012					IOVCC3	
57		P003				AN003	AVCC0	
58		P002				AN002	AVCC0	
59	VREFL0							
60		P001				AN001	AVCC0	
61		P000				AN000	AVCC0	
62	VREFH0/ AVTRO							
63	AVCC0							
64	AVSS0							

Note: Note the following points with regard to pin names.
- For the SCIg interfaces, each communications pin has multiple functions that work differently depending on the mode as follows:
  RXDn/SCLn/MISOn, TXDn/SDAn/MOSIn, CTSn/RTSn/SSn
- We recommend using the sets of pins that have the same letter (“_A”,“_B”,“_C” to indicate group membership) appended to their names.
  For the SPI and SCI interfaces, the AC portion of the electrical characteristics is measured per group.
- Pin functions that have“_DS” appended to their names can be used as inputs for trigger signals for release from deep software standby.

2. CPU

This LSI chip is based on the Arm® Cortex®-M0+ CPU core.

2.1 Overview

2.1.1 CPU

- Arm® Cortex-M0+
  - Revision: r0p1-00rel0
  - Arm®v6-M architecture profile
  - Single-cycle integer multiplier
- Memory Protection Units (MPU)
  - Arm®v6 Protected Memory System Architecture
  - Eight protected regions
- SysTick timer
  - Driven by LOCO clock (32.768 kHz ± 30%)

For details, see reference 1. and reference 2. in section 2.8.

2.1.2 Debug

- Arm® CoreSight™ MTB-M0+
  - Revision: r0p1-00rel0
  - Buffer size: 32-Kbyte MTB RAM
- Data Watchpoint Unit (DWT)
  - Two comparators for watchpoints
- Breakpoint Unit (BPU)
  - Four instruction comparators
- CoreSight Debug Access Port (DAP)
  - Serial Wire Debug Port (SW-DP)
- Debug Register Module (DBGREG)
  - Reset control
  - Stop control

For details, see reference 1. and reference 2. in section 2.8.

2.1.3 Operating Frequency

- CPU core: maximum 64 MHz
- Serial Wire Data (SWD) interface: maximum 12.5 MHz

Figure 2.1 shows the block diagram of the Cortex-M0+ CPU.

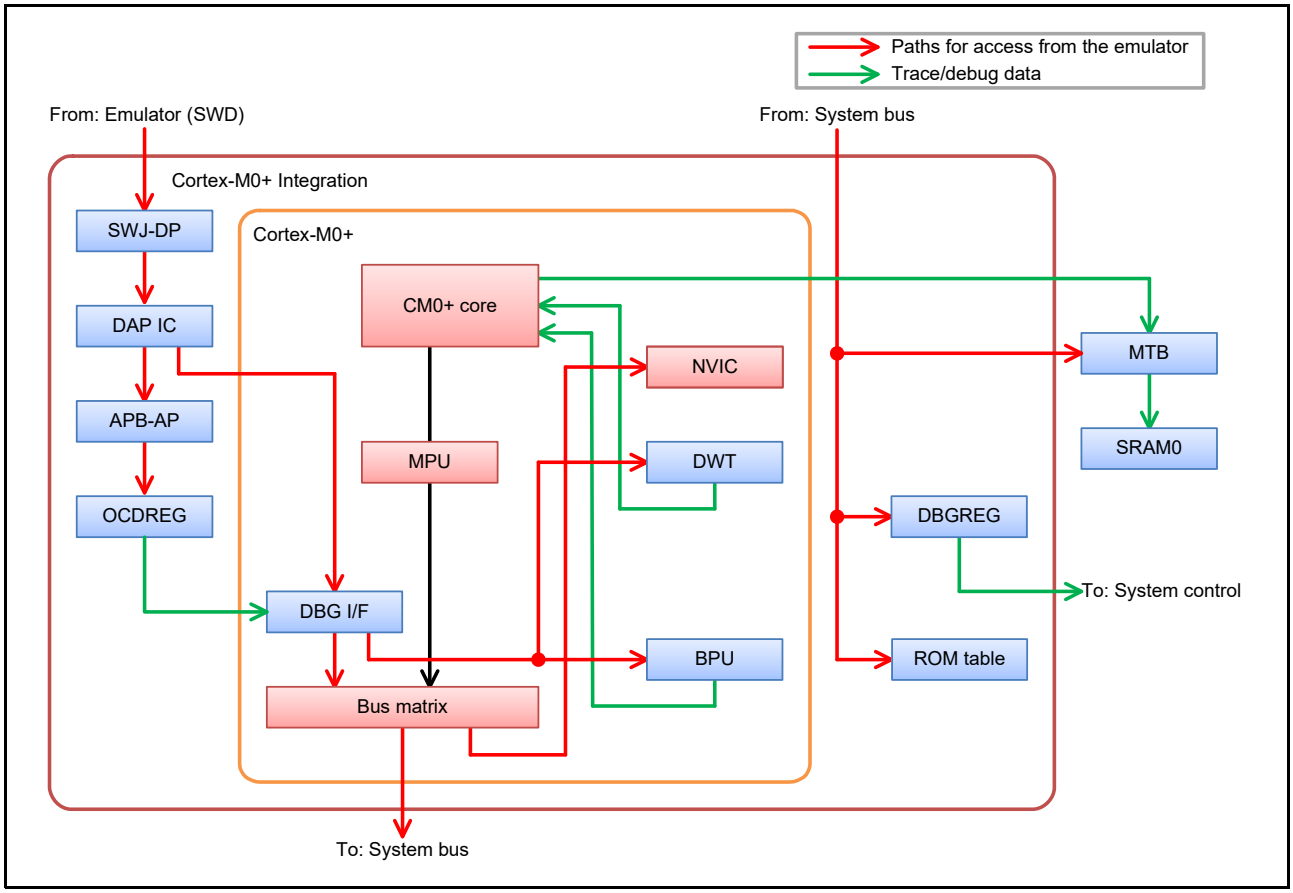


Figure 2.1 Cortex-M0+ CPU Block Diagram

2.2 Implementation Options

Table 2.1 Implementation Options

Option	Implementation
MPU	Included, 8 memory protection regions
Single-cycle multiplier	Included
Number of interrupts	32
Sleep mode power saving	Sleep mode and other low power consumption modes are supported. For details, see section 12, Power-Saving Functions in the User's Manual: Hardware. Note: SCB.SCR.SLEEPDEEP is ignored.
Endianness	Little endian
SysTick timer	See reference 3. in section 2.8.
System reset request output	The SYSRESETREQ bit in the application interrupt and reset control register causes a CPU reset.
Vector table offset register	Included

For details, see reference 3. in section 2.8.

2.3 SWD Interface

The LSI chip supports the SWD interface as a debug interface.
Table 2.2 lists the SWD pins.

Table 2.2 SWD Pins

Pin Name	I/O	Function	When not in Use
SWCLK	Input	Serial wire clock input pin	Pull-up
SWDIO	I/O	Serial wire data I/O pin	Pull-up

2.4 Debug Mode

2.4.1 Debug Mode Definition

Table 2.3 shows the debug modes and conditions.

Table 2.3 Debug Modes and Conditions

Conditions		Mode	
Connection with the Emulator	SWD Authentication	Debug Mode	Debug Authentication
Not connected	—	User mode	Disabled
Connected	Failed	User mode	Disabled
Connected	Passed	On-chip debug (OCD) mode	Enabled

Note: Whether the emulator is connected or not can be determined from the value of the CDBGPWRUPREQ bit in the SWJ-DP register. The bit can only be written by the emulator. Read the DBGSTR.CDBGPWRUPREQ bit to confirm the value of this bit.

Note: Debug authentication is defined by the Arm®v6-M architecture. Enabled means that both invasive and non-invasive CPU debugging are permitted. Disabled means that both of them are not permitted.

2.4.2 Effects of Debug Mode

The debug mode effects occur both internal and external to the CPU. This section describes the effects of the debug mode.

2.4.2.1 Low Power Consumption Mode

All CoreSight debug components can store the register settings even when the CPU enters software standby, snooze, or deep software standby mode. However, AHB-AP cannot respond to on-chip debug (OCD) access in these low power consumption modes. It means the emulator must wait for cancellation of the low power consumption mode to access the CoreSight debug components. In this case, the emulator can request low power consumption mode cancellation by using the DBIRQ bit in the MCUCTRL register. For details, see section 2.5.6.3, MCU Control Register (MCUCTRL).

2.4.2.2 Resets

In OCD mode, the effectiveness of some types of reset depends on the state of the CPU at the time and the settings of bits of the DBGSTOPCR register.

Table 2.4 Reset or Interrupt and Mode Setting

Reset or Interrupt Name	Control in On-chip Debug (OCD) Mode	
	OCD Break Mode	OCD Run Mode
RES# pin reset	Same as user mode	
Power-on reset	Same as user mode	
Independent watchdog timer reset/interrupt	Does not occur*1	Depends on the settings of bits of the DBGSTOPCR register.
Watchdog timer reset/interrupt	Does not occur*1	Depends on the settings of bits of the DBGSTOPCR register.
Voltage monitor 0 reset	Depends on the settings of bits of the DBGSTOPCR register.	
Voltage monitor 1 reset/interrupt	Depends on the settings of bits of the DBGSTOPCR register.	
Voltage monitor BAT reset/interrupt	Depends on the settings of bits of the DBGSTOPCR register.	
Bus master MPU reset/interrupt	Same as user mode	
Bus slave MPU reset/interrupt	Same as user mode	
Stack pointer error reset/interrupt	Same as user mode	
Deep software standby reset	Same as user mode	
MINPWON mode reset	Same as user mode	
Software reset	Same as user mode	

Note: OCD break mode means that the CPU is halted, and OCD run mode means that the CPU is not halted.
Note 1. The IWDT and WDT always stop in OCD break mode.

2.5 Programmers Model

2.5.1 Address Spaces

The debugging system in this LSI chip has two CoreSight Access Ports (AP):

- AHB-AP, which is connected to the CPU bus matrix and has the same access to the system address space as the CPU
- APB-AP, which has a dedicated address space (OCD address space) and is connected to the OCD-dedicated registers.

Figure 2.2 shows the block diagram of the AP connection and address spaces.

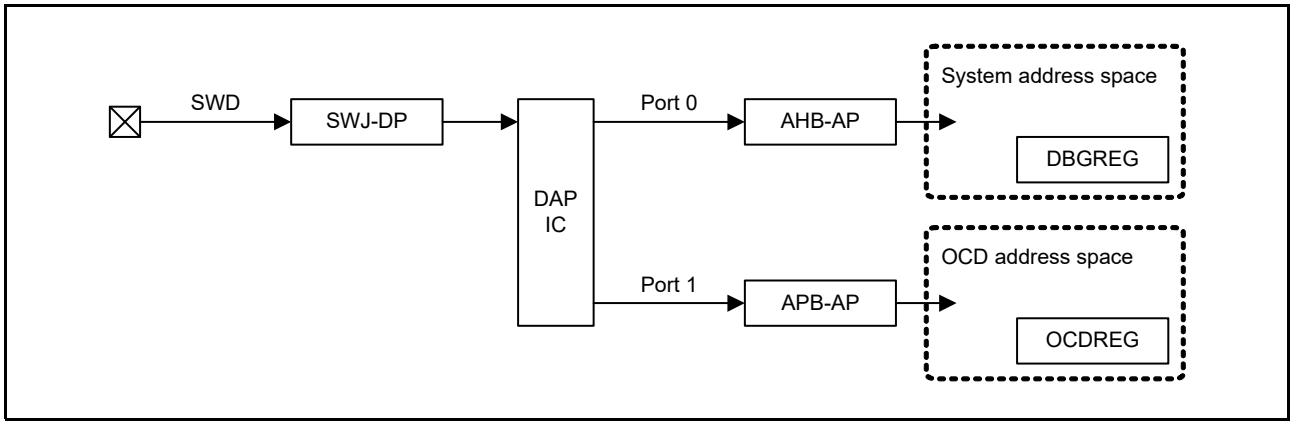


Figure 2.2 Block Diagram of the AP Connection and Address Spaces

For debugging purposes, there are two register modules, DBGREG and OCDREG. DBGREG is located in the system address space and can be accessed from the emulator, the CPU, and other bus masters in the chip. OCDREG is located in the OCD address space and can be accessed only from the emulator. The CPU and other bus masters cannot access the OCD-dedicated registers.

2.5.2 Cortex-M0+ Peripheral Address Map

In system address space, the Cortex-M0+ has a Private Peripheral Bus (PPB), which can be accessed only from the CPU and emulator. Table 2.5 shows the Cortex-M0+ peripheral address map.

Table 2.5 Peripheral Address Map

Component Name	Start Address	End Address	Note
DWT	E000 1000h	E000 1FFFh	See reference 2. in section 2.8.
BPU	E000 2000h	E000 2FFFh	See reference 2. in section 2.8.
SCS	E000 E000h	E000 EEFFh	See reference 2. in section 2.8.
ROM table	E00F F000h	E00F FFFFh	See section 2.5.4, CoreSight ROM Table and reference 5. in section 2.8.

2.5.3 External Debug Address Map

In the system address space, the Cortex-M0+ core has external debug components. These components can be accessed from the CPU and other bus masters through the system bus. Table 2.6 shows the address map of the Cortex-M0+ external debug components.

Table 2.6 Address Map of External Debug Components

Component Name	Start Address	End Address	Note
MTB (RAM area)	2000 0000h	2000 7FFFh	The Micro Trace Buffer (MTB) has 32 Kbytes of available RAM. See reference 6. in section 2.8.
MTB (SFR area)	4001 9000h	4001 9FFFh	See reference 6. in section 2.8.
ROM table	4001 A000h	4001 AFFFh	See reference 6. in section 2.8.

2.5.4 CoreSight ROM Table

This LSI chip has two CoreSight ROM tables. One ROM table holds a list of external debug components and a pointer to Arm® components. The other ROM table holds a list of Arm® components.

2.5.4.1 ROM Entries

Table 2.7 shows the ROM table which contains the pointers to the Arm® system area and user area component information.
Table 2.8 shows the ROM table which contains Arm® system area component information. For details, see references 5. and 6. in section 2.8.

Table 2.7 ROM Table (1)

Address	Access Size	R/W	Value	Target Component
4001 A000h	32 bits	R	A00E 5003h	Arm® Cortex-M0+ processor
4001 A004h	32 bits	R	FFFF F003h	MTB
4001 A008h	32 bits	R	0000 0000h	(End marker for the ROM tables)

Table 2.8 ROM Table (2)

Address	Access Size	R/W	Value	Target Component
E00F F000h	32 bits	R	FFF0 F003h	The SCS is mounted here.
E00F F004h	32 bits	R	FFF0 2003h	The DWT is mounted here.
E00F F008h	32 bits	R	FFF0 3003h	The BPU is mounted here.
E00F F00Ch	32 bits	R	0000 0000h	(End marker for the ROM tables)

2.5.4.2 CoreSight Registers

The CoreSight ROM table has CoreSight registers defined in the Arm® CoreSight architecture. Table 2.9 and Table 2.10 show the registers. See reference 5. in section 2.8 for details on each register.

Table 2.9 CoreSight Registers in the CoreSight ROM Table (Renesas Unique ID)

Name	Address	Access Size	R/W	Initial Value
Arm® CM0+	4001 A000h	32 bits	R	A00E 5003h
MTB	4001 A004h	32 bits	R	FFFF F003h
PID4	4001 AFD0h	32 bits	R	0000 0004h
PID5	4001 AFD4h	32 bits	R	0000 0000h
PID6	4001 AFD8h	32 bits	R	0000 0000h
PID7	4001 AFDCh	32 bits	R	0000 0000h
PID0	4001 AFE0h	32 bits	R	0000 002Ah
PID1	4001 AFE4h	32 bits	R	0000 0030h
PID2	4001 AFE8h	32 bits	R	0000 000Ah
PID3	4001 AFECh	32 bits	R	0000 0000h
CID0	4001 AFF0h	32 bits	R	0000 000Dh
CID1	4001 AFF4h	32 bits	R	0000 0010h
CID2	4001 AFF8h	32 bits	R	0000 0005h
CID3	4001 AFFCh	32 bits	R	0000 00B1h

Table 2.10 CoreSight Registers in the CoreSight ROM Table (CoreSight-ID)

Name	Address	Access Size	R/W	Initial Value
SCS	E00F F000h	32 bits	R	FFF0 F003h
DWT	E00F F004h	32 bits	R	FFF0 2003h
BPU	E00F F008h	32 bits	R	FFF0 3003h
PID4	E00F FFD0h	32 bits	R	0000 0004h
PID5	E00F FFD4h	32 bits	R	0000 0000h
PID6	E00F FFD8h	32 bits	R	0000 0000h
PID7	E00F FFDCh	32 bits	R	0000 0000h
PID0	E00F FFE0h	32 bits	R	0000 00C0h
PID1	E00F FFE4h	32 bits	R	0000 00B4h
PID2	E00F FFE8h	32 bits	R	0000 000Bh
PID3	E00F FFECh	32 bits	R	0000 0000h
CID0	E00F FFF0h	32 bits	R	0000 000Dh
CID1	E00F FFF4h	32 bits	R	0000 0010h
CID2	E00F FFF8h	32 bits	R	0000 0005h
CID3	E00F FFFCh	32 bits	R	0000 00B1h

2.5.5 DBGREG

DBGREG is a register module that controls the debug functions. DBGREG is implemented as a CoreSight-compliant component.

Table 2.11 lists the DBGREG registers excluding the CoreSight registers.

Table 2.11 DBGREG Registers Other than CoreSight

Name		DAP Port	Address	Access Size	R/W
Debug status register	DBGSTR	Port 0	4001 B000h	32 bits	R
Debug stop control register	DBGSTOPCR	Port 0	4001 B010h	32 bits	R/W

2.5.5.1 Debug Status Register (DBGSTR)

Address(es): DBG.DBGSTR 4001 B000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	CDBGPWRUPACK	CDBGPWRUPREQ	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b27 to b0	—	Reserved	These bits are read as 0.	R
b28	CDBGPWRUPREQ	Debug Power-up Request	0: The emulator is not requesting debug power-up. 1: The emulator is requesting debug power-up.	R
b29	CDBGPWRUPACK	Debug Power-up Acknowledge	0: A debug power-up request is being received. 1: A debug power-up request is not being received.	R
b31, b30	—	Reserved	These bits are read as 0.	R

This register is a status register which indicates the state of the debug power-up request to the chip from the emulator.

2.5.5.2 Debug Stop Control Register (DBGSTOPCR)

Address(es): DBG.DBGSTOPCR 4001 B010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	DBGSTOP_LVDBAT	DBGSTOP_LVD1	DBGSTOP_LVD0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DBGSTOP_WDT	DBGSTOP_IWDT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	Bit Name	Description	R/W
b0	DBGSTOP_IWDT	Mask Bit for IWDT Reset/Interrupt	0: Enable IWDT reset/interrupt. 1: Mask IWDT reset/interrupt and stop IWDT count.	R/W
b1	DBGSTOP_WDT	Mask Bit for WDT Reset/Interrupt	0: Enable WDT reset/interrupt. 1: Mask WDT reset/interrupt and stop WDT count.	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	DBGSTOP_LVD0	Mask Bit for LVD0 Reset	0: Enable LVD0 reset. 1: Mask LVD0 reset.	R/W
b17	DBGSTOP_LVD1	Mask Bit for LVD1 Reset/Interrupt	0: Enable LVD1 reset/interrupt. 1: Mask LVD1 reset/interrupt.	R/W
b18	DBGSTOP_LVDBAT	Mask Bit for LVDBAT Reset/Interrupt	0: Enable LVDBAT reset/interrupt. 1: Mask LVDBAT reset/interrupt.	R/W
b31 to b19	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The debug stop control register (DBGSTOPCR) controls certain resets and interrupts in the OCD mode. In user mode, the settings of the bits in this register do not affect the operation of the chip.

2.5.5.3 DBGREG CoreSight Registers

DBGREG has CoreSight registers defined in the Arm® CoreSight architecture. Table 2.12 lists these registers. See reference 5. in section 2.8 for details on each register.

Table 2.12 DBGREG CoreSight Registers

Name	Address	Access Size	R/W	Initial Value
PID4	4001 BFD0h	32 bits	R	0000 0004h
PID5	4001 BFD4h	32 bits	R	0000 0000h
PID6	4001 BFD8h	32 bits	R	0000 0000h
PID7	4001 BFDCh	32 bits	R	0000 0000h
PID0	4001 BFE0h	32 bits	R	0000 0005h
PID1	4001 BFE4h	32 bits	R	0000 0030h
PID2	4001 BFE8h	32 bits	R	0000 001Ah
PID3	4001 BFECh	32 bits	R	0000 0000h
CID0	4001 BFF0h	32 bits	R	0000 000Dh
CID1	4001 BFF4h	32 bits	R	0000 00F0h
CID2	4001 BFF8h	32 bits	R	0000 0005h
CID3	4001 BFFCh	32 bits	R	0000 00B1h

2.5.6 OCDREG

The OCDREG registers are only accessible by the emulator. OCDREG is implemented as a CoreSight-compliant component.
Table 2.13 lists the OCDREG registers.

Table 2.13 OCDREG Registers

Name		DAP Port	Address	Access Size	R/W
ID authentication code register 0	IAUTH0	Port 1	8000 0000h	32 bits	W
ID authentication code register 1	IAUTH1	Port 1	8000 0100h	32 bits	W
ID authentication code register 2	IAUTH2	Port 1	8000 0200h	32 bits	W
ID authentication code register 3	IAUTH3	Port 1	8000 0300h	32 bits	W
MCU status register	MCUSTAT	Port 1	8000 0400h	32 bits	R
MCU control register	MCUCTRL	Port 1	8000 0410h	32 bits	R/W

Note: OCDREG is located in dedicated OCD address space. This address space is independent of the system address space.

2.5.6.1 ID Authentication Code Register (IAUTH0 to IAUTH3)

These registers are authentication registers used for the writing of a 128-bit key. These registers must be written in sequential order from IAUTH0 register to IAUTH3 register.
The initial value of the registers is all FFFF FFFFh. This means that SWD access is initially permitted when ID code in the OSIS register has the initial value. See section 2.7.1, Unlock ID Code.

Address(es): IAUTH0 8000 0000h

b31																														b0
IAUTH0: AID 31-0 bits																														
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Address(es): IAUTH1 8000 0100h

b31																														b0
IAUTH1: AID 63-32 bits																														
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Address(es): IAUTH2 8000 0200h

b31																														b0
IAUTH2: AID 95-64 bits																														
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Address(es): IAUTH3 8000 0300h

b31																														b0
IAUTH3: AID 127-96 bits																														
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

2.5.6.2 MCU Status Register (MCUSTAT)

Address(es): MCUSTAT 8000 0400h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	CPUSTOPCLK	CPUSLEEP	AUTH
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1/0 *1	1/0 *1	0

Bit	Symbol	Bit Name	Description	R/W
b0	AUTH	Debugger Authentication Flag	0: Authentication failed. 1: Authentication succeeded.	R
b1	CPUSLEEP	Sleep Status Flag	0: CPU is not in sleep mode. 1: CPU is in sleep mode.	R
b2	CPUSTOPCLK	Stop Status Flag	0: The clock is being supplied to the CPU. 1: Supply of the clock to the CPU is stopped.	R
b31 to b3	—	Reserved	These bits are read as 0.	R

Note 1. Depends on the state of this chip.

2.5.6.3 MCU Control Register (MCUCTRL)

Address(es): MCUCTRL 8000 0410h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DBIRQ	—	—	—	—	—	—	—	EDBGRQ
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	EDBGRQ	External Debug Request	0: Debug event not requested. 1: Debug event requested. Writing 1 to this bit causes a CPU halt. This bit is cleared by either of the following conditions. • Writing 0 to the EDBGRQ bit • CPU is halted.	R/W
b7 to b1	—	Reserved	These bits are read as 0.	R
b8	DBIRQ	Debug Interrupt Request	0: Debug interrupt not requested. 1: Debug interrupt requested. Writing 1 to this bit wakes up the chip from low power consumption mode.	R/W
b31 to b9	—	Reserved	These bits are read as 0.	R

Note: Set the DBIRQ and EDBGRQ bits to the same value.

2.5.6.4 OCDREG CoreSight Registers

OCDREG has CoreSight registers defined in the Arm® CoreSight architecture.
Table 2.14 lists these registers. See reference 5. in section 2.8 for details on each register.

Table 2.14 OCDREG CoreSight Registers

Name	Address	Access Size	R/W	Initial Value
PID4	8000 0FD0h	32 bits	R	0000 0004h
PID5	8000 0FD4h	32 bits	R	0000 0000h
PID6	8000 0FD8h	32 bits	R	0000 0000h
PID7	8000 0FDCh	32 bits	R	0000 0000h
PID0	8000 0FE0h	32 bits	R	0000 0004h
PID1	8000 0FE4h	32 bits	R	0000 0030h
PID2	8000 0FE8h	32 bits	R	0000 000Ah
PID3	8000 0FECh	32 bits	R	0000 0000h
CID0	8000 0FF0h	32 bits	R	0000 000Dh
CID1	8000 0FF4h	32 bits	R	0000 00F0h
CID2	8000 0FF8h	32 bits	R	0000 0005h
CID3	8000 0FFCh	32 bits	R	0000 00B1h

2.6 SysTick Timer

This LSI chip has a SysTick timer that provides a simple 24-bit down counter. The timer can select ICLK or SYSTICCLK reference clock.
For details, see section 9, Clock Generation Circuit in the User's Manual: Hardware and reference 1. in section 2.8.

2.7 Connection with the Emulator

This LSI chip has an SWD authentication mechanism to check permission for access to chip resources for debugging. Permission for full debug functionality requires passing the authentication process.
Figure 2.3 shows the block diagram of the authentication mechanism.

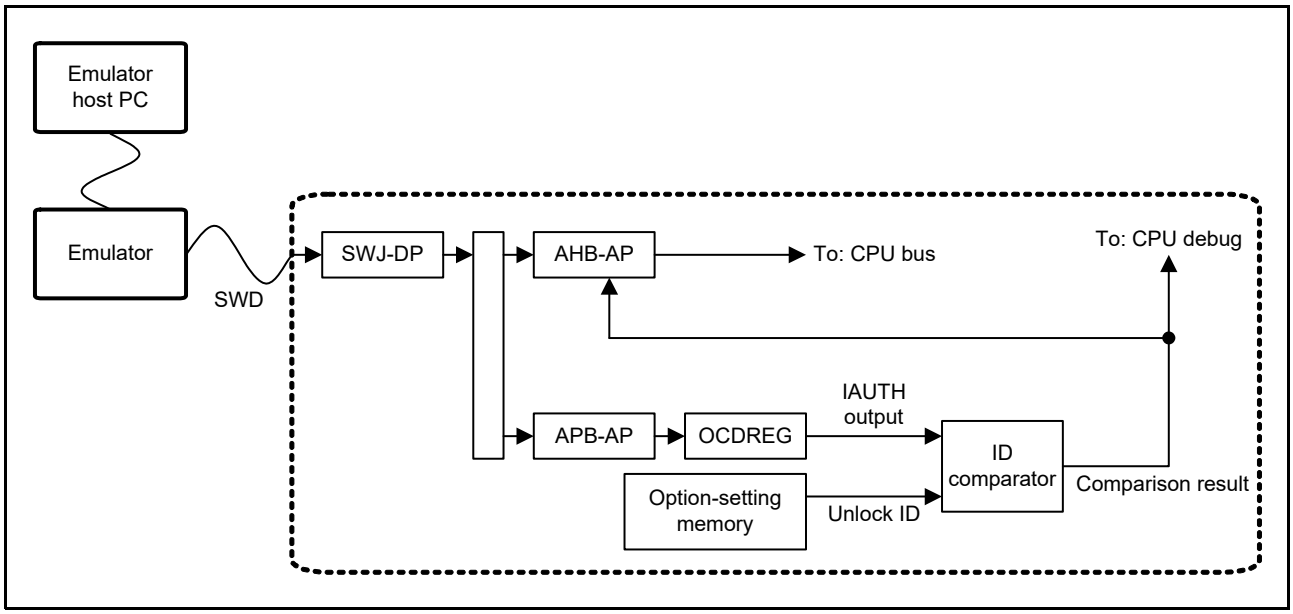


Figure 2.3 SWD Authentication Mechanism Block Diagram

The LSI chip includes an ID comparator for use in SWD authentication. The comparator compares the 128-bit IAUTH output value from the given registers in the OCDREG space with the 128-bit unlock ID code written in the OCD/serial programmer ID setting register (OSIS) in the option-setting memory. The two outputs being identical represents a pass in SWD authentication and use of the CPU debug functions and system bus access from the emulator are permitted. After passing SWD authentication, the emulator must set the DBGEN bit in the system control OCD control register (SYOCDCR). In addition, the emulator must clear the DBGEN bit before disconnection. See the description of the SYOCDCR register in section 12, Power-Saving Functions in the User's Manual: Hardware.

2.7.1 Unlock ID Code

The unlock ID code is used for checking permissions for the CPU debug functions and system bus access. If the unlock ID code matches the 128-bit data written in the IAUTH0 to IAUTH3 registers, the SWD debugger obtains access permission. Unlock ID code is written in the OCD/serial programmer ID setting register (OSIS) in the option-setting memory. The initial value of the unlock ID code is all 1s (FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFFh). For details on the OSIS register, see section 7, Option-Setting Memory in the User's Manual: Hardware.

2.7.2 Restrictions on Connecting an Emulator

To start a SWD connection from an emulator, the chip must be able to enter OCD mode. To do so, however, there are some restrictions depending on the current chip state. Table 2.15 lists in which mode and power consumption state the chip can transition to OCD mode.
Since the chip cannot transition to OCD mode while in EXFPWON and normal modes, MINPWON and normal modes, or VBB mode, change the chip to OCD mode while in ALLPWON and normal modes, and then change it to EXFPWON and normal modes, MINPWON and normal modes, or VBB mode in order to carry out debugging in EXFPWON and normal modes, MINPWON and normal modes, or VBB mode. For details, see section 12, Power-Saving Functions in the User's Manual: Hardware.

Table 2.15 State of the LSI Chip That can Transition to OCD Mode

Current Operating Mode before Transitioning to OCD Mode			Transition to OCD Mode
Power Control Mode	Power Supply Mode	Low Power Consumption Modes	
Boost mode	—	Operating mode	Possible*1
		Sleep mode	Possible*1
Normal mode	ALLPWON mode	Operating mode	Possible*1
		Sleep mode	Possible*1
		Snooze mode	Impossible
		Software standby mode	Impossible
		Deep software standby mode	Impossible
	EXFPWON mode MINPWON mode	All modes	Impossible
VBB mode	ALLPWON mode EXFPWON mode MINPWON mode	All modes	Impossible
Mode transition period			Impossible

Note 1. After transition to the OCD mode, set 1 to the SYOCDCR.DBGEN bit (on-chip debugger enable). For details on the SYOCDCR.DBGEN bit, see section 12.2.22, System Control OCD Control Register (SYOCDCR) in the User's Manual: Hardware.

2.7.2.1 Mode Transitions while in OCD Mode

Some restrictions apply to mode transitions while in OCD mode. Table 2.16 lists availability of mode transitions between the power control modes.

Table 2.16 Availability of Mode Transitions between the Power Control Modes while in OCD Mode

Current Power Control Mode	Power Control Mode to Transition to	Availability of Mode Transitions between the Power Control Modes
Boost mode	Normal mode	Impossible
Normal mode	Boost mode	Impossible
	VBB mode	Possible*1, *2
VBB mode	Normal mode	Possible*1

Note 1. Although power control mode transition between normal and VBB modes is possible, the state of the power in normal mode is maintained in order to continue debugging. Functions such as state flagging can be emulated.
Note 2. After transition to the OCD mode while in ALLPWON and normal modes, set the SYOCDCR.DBGEN bit to 1 (on-chip debugger enable) before transition to the VBB mode. For details on the SYOCDCR.DBGEN bit, see section 12.2.22, System Control OCD Control Register (SYOCDCR) in the User's Manual: Hardware.

After transition to the OCD mode while in ALLPWON and normal modes, set the SYOCDCR.DBGEN bit to 1 (on-chip debugger enable) before transition to EXFPWON or MINPWON mode. For details on the SYOCDCR.DBGEN bit, see section 12.2.22, System Control OCD Control Register (SYOCDCR) in the User's Manual: Hardware.

2.7.2.2 Entering Low Power Consumption Mode while in OCD Mode

The chip can enter low power consumption mode even while it is in OCD mode.
After transition to the OCD mode, set the SYOCDCR.DBGEN bit to 1 (on-chip debugger enable) before transition to low power consumption mode. For details on the SYOCDCR.DBGEN bit, see section 12.2.22, System Control OCD Control Register (SYOCDCR) in the User's Manual: Hardware.

If system bus access is required and the chip is in software standby, snooze, or deep software standby mode, set the MCUCTRL.DBIRQ bit in OCDREG to 1 to wake the chip up from the low power consumption mode. Simultaneously, using the MCUCTRL.EDBGRQ bit in OCDREG, the emulator can wake up the chip without starting CPU execution. Table 2.17 lists availability of access to system bus while in OCD mode.

Table 2.17 Availability of Access to System Bus while in OCD Mode

Current Mode	Current Low Power Consumption Mode	Access to System Bus
Boost mode	Operating mode	Possible
	Sleep mode	Possible
Normal mode	Operating mode	Possible
	Sleep mode	Possible
	Snooze mode	Impossible
	Software standby mode	Impossible
	Deep software standby mode	Impossible
VBB mode	Operating mode	Possible
	Sleep mode	Possible
	Snooze mode	Impossible
	Software standby mode	Impossible
	Deep software standby mode	Impossible
Mode transition period		Impossible

2.7.2.3 Modifying the Unlock ID Code in the OSIS Register

Modifying the unlock ID code in the OSIS register requires placing the chip in the reset state by asserting the signal on the RES# pin or setting the SYSRESETREQ bit of the application interrupt and reset control register in the system control block to 1. The modified unlock ID code is reflected after the reset. For the system control block, see reference 2. listed in section 2.8.
The emulator must set the modified unlock ID code in the IAUTH0 to IAUTH3 registers immediately before the chip is placed in the reset state. When the IAUTH0 to IAUTH3 registers have been overwritten, writing to the SYSRESETREQ bit is not possible. Place the chip in the reset state by asserting the signal on the RES# pin.

2.7.2.4 Connecting Sequence and SWD Authentication

Protection of the connection with the emulator by the SWD authentication mechanism means that input of an unlock ID code to the SWD authentication registers will be required in some cases. The value for the OSIS register in the option-setting memory decides whether the input of an unlock ID code is required or not. After de-asserting the signal on the RES# pin, a waiting time is required before comparison with the OSIS register value following cold start. For the waiting time after de-assertion of the signal on the RES# pin, see section 6.3.3, Reset Timing in section 6, Electrical Characteristics.
The SWD authentication process is described in detail below.

(1) When MSB of the OSIS register is 0 (bit 127 = 0)

The ID code is always mismatching, and the connection to the emulator is prohibited.

(2) When bits in the OSIS register are all 1s (the initial value)

ID authentication is not required and the emulator can use AHB-AP without the authentication.

For details of the settings for using the AHB-AP, see reference 4. in section 2.8.

1. Connect the emulator to the chip through the SWD interface.
2. Set up SWJ-DP to access the DAP bus. In the setup, the emulator must assert CDBGPWRUPREQ in the SWJ-DP control status register, then must wait until CSDBGPWRUPACK in the same register is asserted.
3. Set up AHB-AP to access the system address space. AHB-AP is connected to the DAP bus port 0.
4. Start accessing the system bus using AHB-AP.

(3) When the value in the OSIS register becomes “ALeRASE” in ASCII code

Data in the flash memory are deleted. For details, see section 48, Flash Memory in the User’s Manual: Hardware.

1. Set the ASCII code “ALeRASE” (414C 6552 4153 45FF FFFF FFFF FFFF FFFFh) in the IAUTH0 to IAUTH3 registers.
2. Place the chip in the reset state.
3. Wait until MCUSTAT.CPUSTOPCLK = 1 (deletion completed).
4. Reset the chip then release it from the reset state so that it enters the OCD mode.
5. Confirm that all bits of the unlock ID code are 1 (the code is FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFFh).

(4) When bits in the OSIS register are not all 1s

ID authentication is required and the emulator must write the 128-bit unlock ID code to the IAUTH0 to IAUTH3 registers in OCDREG before using AHB-AP.

1. Connect the emulator to the chip through the SWD interface.
2. Set up the SWJ-DP to access the DAP bus. In the setup, the emulator must assert CDBGPWRUPREQ in the SWJ-DP control status register, then wait until CSDBGPWRUPACK in the same register is asserted.
3. Set up APB-AP to access OCDREG. APB-AP is connected to the DAP bus port 1.
4. Write the 128-bit unlock ID code to the IAUTH0 to IAUTH3 registers in OCDREG using APB-AP.
5. If the 128-bit unlock ID code matches the OSIS register value, AHB-AP is authorized to issue an AHB transaction. The authentication result can be confirmed in the AUTH bit in the MCUSTAT register or the DbgStatus bit in the AHB-AP control status word register.
   - When the DbgStatus bit is 1, the 128-bit ID code is a match with the OSIS value. AHB transfers are permitted.
   - When the DbgStatus bit is 0, the 128-bit ID code is not a match with the OSIS value. AHB transfers are not permitted.
6. Set up AHB-AP to access the system address space. AHB-AP is connected to the DAP bus port 0.
7. Start accessing the CPU debug resources using AHB-AP.

2.8 References

1. ARM® v6-M Architecture Reference Manual (ARM DDI 0419E)
2. Cortex™-M0+ Technical Reference Manual (ARM DDI 0484C)
3. Cortex™-M0+ Devices Generic User Guide (ARM DUI 0662B)
4. Arm® CoreSight™ SoC-400 Technical Reference Manual (ARM DDI 0480G)
5. Arm® CoreSight™ Architecture Specification (ARM IHI 0029E)
6. CoreSight™ MTB-M0+ Technical Reference Manual (ARM DDI 0486B)

3. Startup Modes

3.1 Types and Selection of Startup Mode

Table 3.1 shows the startup modes selected by the levels on the mode setting pins (MD and EHMD). For details on each of the startup modes, see section 3.2, Details of Startup Modes.

Table 3.1 Types of Startup Mode Selected by the Levels on the Startup Mode Setting Pin and Energy Harvesting Mode Setting Pin

Mode Setting Pins		Startup Mode
MD	EHMD	
High	High	Energy harvesting startup mode
	Low	Normal startup mode
Low	—	SCI boot mode

3.2 Details of Startup Modes

3.2.1 Normal Startup and Energy Harvesting Startup Modes

In normal startup and energy harvesting startup modes, all input and output pins are available for use as input or output ports, inputs or outputs for peripheral functions, or as interrupt inputs. When release from the reset state proceeds while the MD pin is high, the LSI chip starts in normal startup or energy harvesting startup mode and starts running the program in the code flash memory. The EHMD pin can be used to select normal startup or energy harvesting startup. For details, see section 3.3.2, Power-up Sequence.

3.2.2 Serial Programming Mode

3.2.2.1 SCI Boot Mode

In this mode, the code flash memory modifying program (boot program) stored in a dedicated area within the chip is started up. The code flash memory can be modified from outside the chip by using the asynchronous interface. For details, see section 48, Flash Memory in the User's Manual: Hardware.
The LSI chip starts in the serial programming mode if the MD pin is held low on release from the reset state. After the LSI chip has been started up in the serial programming mode, the boot program starts up the asynchronous interface.

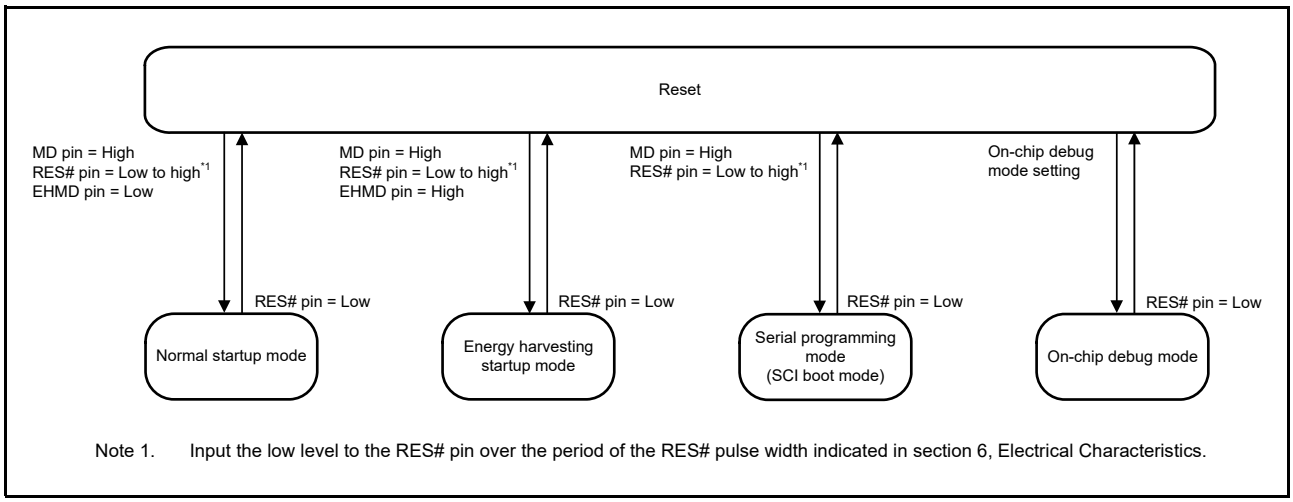
3.2.3 On-chip Debug Mode

In this mode, the chip can be externally controlled by connecting an external emulator or flash memory programmer through the SWD interface.

3.3 Startup Mode Transitions

3.3.1 Startup Mode Determined by the Mode Setting Pins

Figure 3.1 shows startup mode transitions determined by the settings of the MD pin and the EHMD pin.



Note 1. Input the low level to the RES# pin over the period of the RES# pulse width indicated in section 6, Electrical Characteristics.

Figure 3.1 Startup Mode Determined by Levels on the Startup Mode Setting Pin and Energy Harvesting Mode Setting Pin

3.3.2 Power-up Sequence

The normal startup or energy harvesting startup mode is selected by the state of the EHMD pin on release from the reset state as shown in Table 3.2.

Table 3.2 Types of Startup Mode Selected by the State of the EHMD Pin

EHMD Pin State	Startup Mode
Low	Normal startup mode
High	Energy harvesting startup mode

The procedure for using the low leakage current mode as one of power control modes depends on the selected startup mode.

In the normal startup mode, the LSI chip starts with the back bias voltage control (VBBC) circuit disabled. Using the low leakage current mode after normal startup requires waiting for completion of the startup setting and initial setup of the VBBC circuit after release from the internal reset state. The initial setup of the VBBC circuit is the operation of charging an external capacitor connected between VBP and VBN. Setting the back bias voltage control (VBBC) enable bit (VBBCR.VBBEN) to 1 starts this initial setup. When the initial setup is completed, the back bias voltage control (VBBC) initial setup completion flag (VBBST.VBBSTUP) is set to 1. Transition to the low leakage current mode becomes possible when the VBBST.VBBSTUP flag is 1.

In the energy harvesting startup mode, the initial setup of the VBBC circuit starts and is completed during the internal reset period. Consequently, the chip can enter the low leakage current mode immediately, since the VBBCR.VBBEN bit and the VBBST.VBBSTUP flag will be 1 at the time of release from the internal reset state. Although the internal reset period for the energy harvesting startup mode is longer than that for the normal startup mode, the amount of current drawn is reduced during the initial setup of the VBBC circuit.

For details on the low leakage current mode, see section 12, Power-Saving Functions in the User's Manual: Hardware.

4. Address Space

4.1 Address Space

This LSI chip supports a 4-Gbyte linear address space from 0000 0000h to FFFF FFFFh, that can contain both programs and data.

Figure 4.1 shows the memory map.

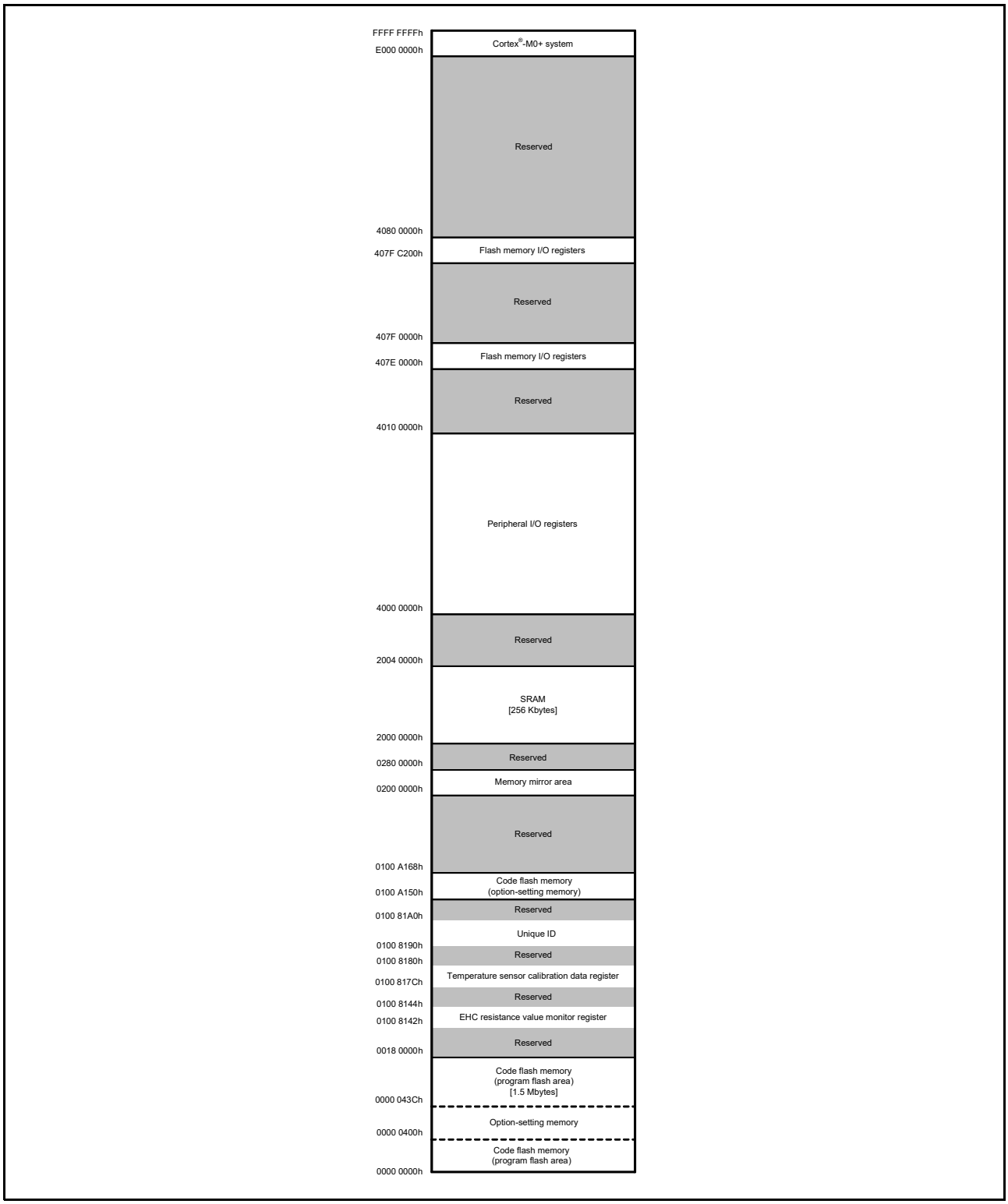


Figure 4.1 Memory Map

5. I/O Registers

This section describes I/O register addresses and access cycles by function.

5.1 Address Information

Table 5.1 lists the address information for I/O registers in this product.

Table 5.1 I/O Register Address (1/2)

Start Address	End Address	Module Symbol	Description
4000 0000h	4000 4FFFh	MPU, MMF, BUS	Memory Protection Unit, memory mirror function, bus control
4000 5000h	4000 5FFFh	DMAC, DTC	DMA controller, data transfer controller
4000 6000h	4000 6FFFh	ICU	Interrupt controller
4001 9000h	4001 9FFFh	MTB	Debug function (MTB)
4001 A000h	4001 AFFFh	FLASH	Flash memory
4001 B000h	4001 BFFFh	DBG	Debug function
4001 E000h	4001 EFFFh	SYSTEM	System control
4004 0000h	4004 001Fh	PORT0	Port 0 control register
4004 0020h	4004 003Fh	PORT1	Port 1 control register
4004 0040h	4004 005Fh	PORT2	Port 2 control register
4004 0060h	4004 007Fh	PORT3	Port 3 control register
4004 0080h	4004 009Fh	PORT4	Port 4 control register
4004 00A0h	4004 00BFh	PORT5	Port 5 control register
4004 00C0h	4004 00DFh	PORT6	Port 6 control register
4004 00E0h	4004 00FFh	PORT7	Port 7 control register
4004 0800h	4004 0CFFh	PFS	Port mn pin function select register
4004 0D00h	4004 0FFFh	PMISC	Miscellaneous port control register
4004 1000h	4004 10FFh	ELC	Event link controller
4004 1240h	4004 125Fh	SCI2	Serial communication interface 2
4004 1260h	4004 127Fh	SCI3	Serial communication interface 3
4004 2000h	4004 20FFh	POE0	Port output enable 0
4004 2100h	4004 21FFh	POE1	Port output enable 1
4004 4000h	4004 40FFh	RTC	Realtime clock
4004 4200h	4004 42FFh	WDT	Watchdog timer
4004 4400h	4004 44FFh	IWDT	Independent watchdog timer
4004 4600h	4004 46FFh	CAC	Clock frequency accuracy measurement circuit
4004 7000h	4004 70FFh	MSTP	Module stop control registers B, C, D
4005 2000h	4005 207Fh	TMR	8-bit timer
4005 3100h	4005 31FFh	RIIC1	I^2C bus interface 1
4005 4100h	4005 41FFh	DOC	Data operation circuit
4005 5000h	4005 50FFh	GPT320	General PWM timer 0 (32 bits)
4005 5300h	4005 53FFh	GPT163	General PWM timer 3 (16 bits)
4005 C000h	4005 C1FFh	S14AD	14-bit A/D converter
4005 D000h	4005 D0FFh	TEMPS	Temperature sensor
4007 0800h	4007 0DFFh	GDT	2D graphics data conversion circuit
4007 2100h	4007 21FFh	SPI1	Serial peripheral interface 1 (32 bits)
4007 4000h	4007 40FFh	CRC	CRC calculator
4008 0000h	4008 00FFh	KINT	Key interrupt function

Table 5.1 I/O Register Address (2/2)

Start Address	End Address	Module Symbol	Description
4008 0400h	4008 04FFh	CCC	Clock correction circuit
4008 4000h	4008 40FFh	AGT0	Asynchronous general-purpose timer 0
4008 4100h	4008 41FFh	AGT1	Asynchronous general-purpose timer 1
4008 4400h	4008 44FFh	LST	Low-speed clock timer
4008 4500h	4008 457Fh	DIL	Data inversion circuit
4008 4680h	4008 46FFh	DIV	Divider
4008 6A80h	4008 6AFFh	VREF	Reference voltage generation circuit
400C 0000h	400C 01FFh	TSIP-Lite	Security function

5.2 Access Cycle

Table 5.2 lists the access cycle information of the I/O registers in this LSI chip. The following statements apply to Table 5.2:

- Registers are grouped by corresponding modules.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the I/O register area, reserved addresses that are not allocated to registers must not accessed. If access is attempted, further operation cannot be guaranteed.
- The number of access cycles for I/O registers depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency between ICLK and PCLK. “PCLK” refers to both PCLKA and PCLKB. For the internal peripheral bus, see section 18, Buses in the User’s Manual: Hardware.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, 1 cycle of PCLK is added to the divided clock synchronization cycles.
- The numbers of cycles are applicable when access by the CPU does not conflict with bus access by another bus master (the DMAC or DTC).

Table 5.2 I/O Register Access Cycle (1/2)

Function	Start Address	End Address	ICLK = PCLK		ICLK > PCLK*1		Cycle Unit	Related Function
			Read	Write	Read	Write		
CPU, MPU, MMF, Bus, DMAC, DTC, ICU, FLASH, DBG	4000 0000h	4000 6FFFh	3	3	—	—	ICLK	CPU, Memory Protection Unit, memory mirror function, bus control, DMA controller, data transfer controller, interrupt controller, flash memory, debug function
	4001 A000h	4001 BFFFh			—	—		
MTB	4001 9000h	4001 9FFFh	2	2	—	—	ICLK	Debug function (MTB)
System control*3	4001 E000h	4001 E3FFh	3	3	—	—	ICLK	Low power consumption function, resets, clock generation function, register write protection function, low voltage detection, energy harvesting control circuit
	4001 E400h	4001 E412h	5	5	—	—		
	4001 E413h	4001 E413h	3	3	—	—		
	4001 E414h	4001 E420h	5	5	—	—		
	4001 E421h	4001 E421h	3	3	—	—		
	4001 E422h	4001 E4E0h	5	5	—	—		
	4001 E4E1h	4001 E4E1h	3	3	—	—		
	4001 E4E2h	4001 E4FFh	5	5	—	—		
	4001 E500h	4001 EFFFh	3	3	—	—		
GPIO*4	4004 0000h	4004 10FFh	3	3	2-3	2-3	PCLKB	I/O ports, event link controller
SCI2 and SCI3	4004 1240h	4004 127Fh	3	3	2-3*2	2-3*2	PCLKB	Serial communications interface
POE0 and POE1	4004 2000h	4004 21FFh	3	3	2-3	2-3	PCLKB	Port output enable
RTC, WDT, IWDT, CAC, MSTP	4004 4000h	4004 70FFh	3	3	2-3	2-3	PCLKB	Realtime clock, watchdog timer, independent watchdog timer, clock frequency accuracy measurement circuit, module stop control
TMR	4005 2000h	4005 207Fh	3	3	2-3	2-3	PCLKB	8-bit timer
RIIC1	4005 3100h	4005 31FFh	3	3	2-3	2-3	PCLKB	I2C bus interface
DOC	4005 4100h	4005 41FFh	3	3	2-3	2-3	PCLKB	Data operation circuit
GPT0*5	4005 5000h	4005 50FFh	6	4	5-6	3-4	PCLKB	General PWM timer 0

Table 5.2 I/O Register Access Cycle (2/2)

Function	Start Address	End Address	ICLK = PCLK		ICLK > PCLK*1		Cycle Unit	Related Function
			Read	Write	Read	Write		
GPT3*6	4005 5300h	4005 53FFh	6	4	5-6	3-4	PCLKB	General PWM timer 3
S14AD	4005 C000h	4005 C1FFh	3	3	2-3	2-3	PCLKB	14-bit A/D converter
TEMPS	4005 D000h	4005 D0FFh	3	3	2-3	2-3	PCLKB	Temperature sensor
GDT	4007 0800h	4007 0DFFh	3	3	—	—	PCLKA	2D graphics data conversion circuit
SPI1	4007 2100h	4007 21FFh	3	3	—	—	PCLKA	Serial peripheral interface
CRC	4007 4000h	4007 40FFh	3	3	—	—	PCLKA	CRC calculator
KINT	4008 0000h	4008 00FFh	3	3	2-3	2-3	PCLKB	Key interrupt function
CCC	4008 0400h	4008 04FFh	4	4	3-4	3-4	PCLKB	Clock correction circuit
AGT0 and AGT1	4008 4000h	4008 41FFh	4	4	3-4	3-4	PCLKB	Asynchronous general-purpose timer
LST	4008 4400h	4008 44FFh	4	4	3-4	3-4	PCLKB	Low-speed clock timer
DIL	4008 4500h	4008 457Fh	4	4	3-4	3-4	PCLKB	Data inversion circuit
DIV	4008 4680h	4008 46FFh	4	4	3-4	3-4	PCLKB	Divider
VREF	4008 6A80h	4008 6AFFh	4	4	3-4	3-4	PCLKB	Reference voltage generation circuit
TSIP-Lite	400C 0000h	400C 01FFh	3	3	—	—	PCLKA	Security function

Note 1. If the number of PCLK cycles is a non-integer (for example 1.5), the minimum value is rounded down to an integer, and the maximum value is rounded off to an integer. For example, 1.5 to 2.5 is 1 to 3.
Note 2. When accessing a 16-bit register (CDR), the time required to access is 2 cycles more than the value shown in Table 5.2.
Note 3. These values indicate the minimum numbers of cycles for access by the CPU. They do not include the cycles required for changes in the source of the ICLK clock and frequency after changes to the SCKSCR and SCKDIVCR registers.
Note 4. GPIO indicates PORT0 to PORT7, PFS, PMISC, and the ELC.
Note 5. GPT0 refers to GPT320.
Note 6. GPT3 refers to GPT163.

6. Electrical Characteristics

The electrical characteristics of the LSI chip are defined under the following conditions unless otherwise specified:

VCC = AVCC0 = IOVCC0 = IOVCC1 = IOVCC2 = IOVCC3 = 1.62 to 3.6 V
1.62 V ≤ VREFH0 ≤ AVCC0
VSS = AVSS0 = VREFL0 = 0 V
$T_a = T_{opr}$
The load capacitance of each I/O pin is 30 pF.
When measuring the power consumption, low CL4 (SOMCR.SODRV = 1 and SOMCR.SODRV0 = 0) was selected for the driving ability of the sub-clock oscillator.

6.1 Absolute Maximum Ratings

Table 6.1 Absolute Maximum Ratings

Item		Symbol	Value	Unit
Power supply voltage	Power supply voltage	VCC	–0.3 to 4.0	V
	Input voltage for EHC	VSC_VCC	–0.3 to 4.0	V
	Secondary battery input voltage for EHC	VBAT_EHC	–0.3 to 4.0	V
	Power supply voltage for I/O pins	IOVCC, IOVCC0 to IOVCC3	–0.3 to 4.0	V
Input voltage	ANT	V_{in}	–1.0 to +1.4	V
	XTAL1_RF, XTAL2_RF		–0.3 to +1.4	V
	DCLIN_A, DCLIN_D		–0.3 to +2.2	V
	Other than above		–0.3 to VCC + 0.3 (max. 4.0 V)	V
Reference power supply voltage		VREFH0	–0.3 to AVCC0 + 0.3 (max. 4.0 V)	V
		VREFL0	–0.3 to AVSS0 + 0.3	V
Analog power supply voltage		AVCC0	–0.3 to 4.0	V
Junction temperature		T_j	–40 to +95	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the LSI chip might result if absolute maximum ratings are exceeded.

Table 6.2 Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	VCC	1.62	—	3.6	V
	VSS	—	0	—	V
Input voltage for EHC	VSC_VCC	1.62	—	3.6	V
Secondary battery input voltage for EHC	VBAT_EHC*1	1.62	—	3.6	V
Analog power supply voltage	AVCC0	1.62	—	3.6	V
	AVSS0	—	0	—	V
	VREFH0	1.62	—	AVCC0	V
	VREFL0	—	0	—	V
Power supply voltage for I/O pins	IOVCC, IOVCC0, IOVCC1, IOVCC2, IOVCC3	1.62	—	3.6	V
BLE power supply voltage	VCC_RF, AVCC_RF	1.8	—	3.6	V
	VSS_RF	—	0	—	V
Operating temperature	T_{opr}	–40	—	85	°C

Note 1. The voltage of the secondary battery to be connected to VBAT_EHC is 2.6 V or 3.0 V.

6.2 DC Characteristics

6.2.1 Input Characteristics of I/O Pins (V_{IH} and V_{IL})

Table 6.3 Input Characteristics of I/O Pins (V_{IH} and V_{IL})

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RES#, NMI, and IRQ pins and input pins of on-chip peripheral functions other than those of the RIIC	V_{IH}	VCC × 0.8	—	—	V	—
		V_{IL}	—	—	VCC × 0.2		
		ΔV_T	0.3	—	—		
	RIIC	V_{IH}	VCC × 0.7	—	—		VCC = 3.0 to 3.6 V
		V_{IL}	—	—	VCC × 0.3		
		ΔV_T	VCC × 0.05	—	—		
Input voltage other than that for the Schmitt trigger input pins	EXTAL, MD, EHMD, and general-purpose I/O ports	V_{IH}	VCC × 0.8	—	—		—
		V_{IL}	—	—	VCC × 0.2		

6.2.2 Output Characteristics of I/O Pins (V_{OH} and V_{OL}) (1)

Table 6.4 Output Characteristics of I/O Pins (V_{OH} and V_{OL})

Item	Setting of the Register	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high-level voltage	Low driving ability (PmnPFS.DSCR[1:0] = 00b)	V_{OH}	VCC – 0.5	—	—	V	I_{OH} = 10 µA
	Middle driving ability (PmnPFS.DSCR[1:0] = 01b)		VCC – 0.5	—	—		I_{OH} = 10 µA
	Standard driving ability (PmnPFS.DSCR[1:0] = 10b)		VCC – 0.6	—	—		I_{OH} = 2 mA
	High driving ability (PmnPFS.DSCR[1:0] = 11b)		VCC – 0.5	—	—		I_{OH} = 2 mA
Output low-level voltage	Low driving ability (PmnPFS.DSCR[1:0] = 00b)	V_{OL}	—	—	0.5		I_{OL} = 2 mA
	Middle driving ability (PmnPFS.DSCR[1:0] = 01b)		—	—	0.5		I_{OL} = 2 mA
	Standard driving ability (PmnPFS.DSCR[1:0] = 10b)		—	—	0.6		I_{OL} = 2 mA
	High driving ability (PmnPFS.DSCR[1:0] = 11b)		—	—	0.5		I_{OL} = 2 mA

Table 6.5 Conditions for Testing I/O Characteristics

	Typ. 33	Typ. 18	Min.	Unit
VCC	3.3	1.8	1.6	V
Temperature	25	25	125	°C

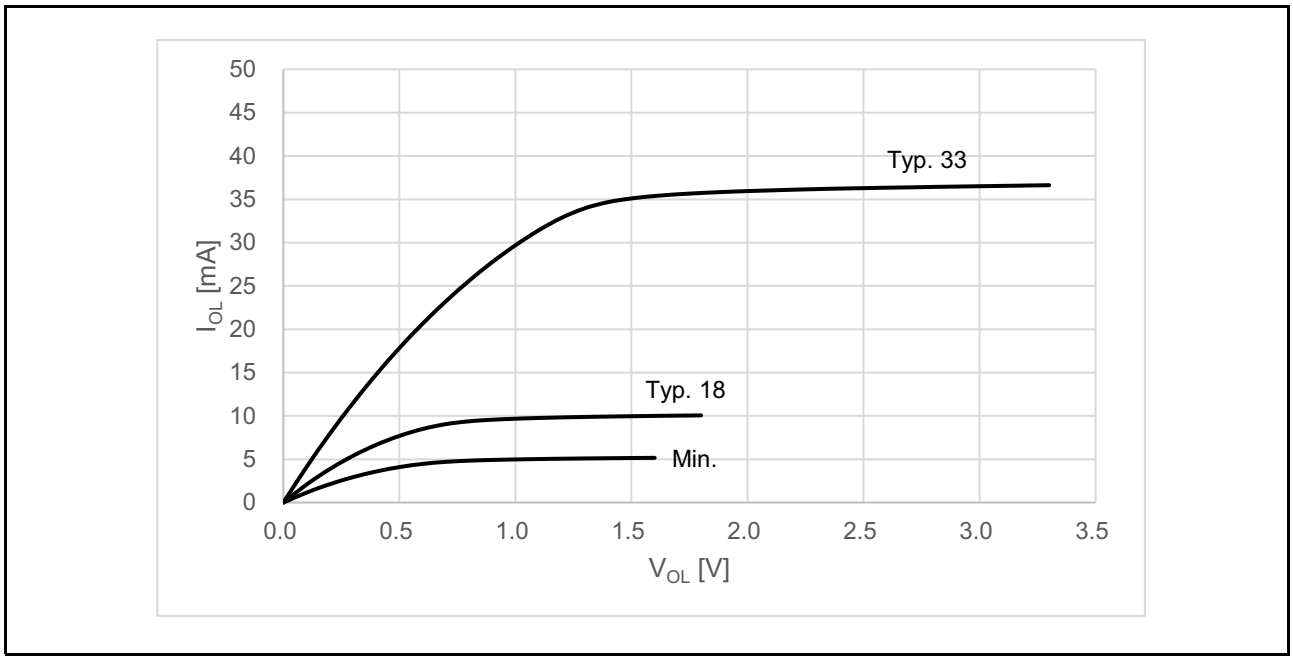


Figure 6.1 V_{OL} vs. I_{OL} Characteristics (Low Driving Ability)

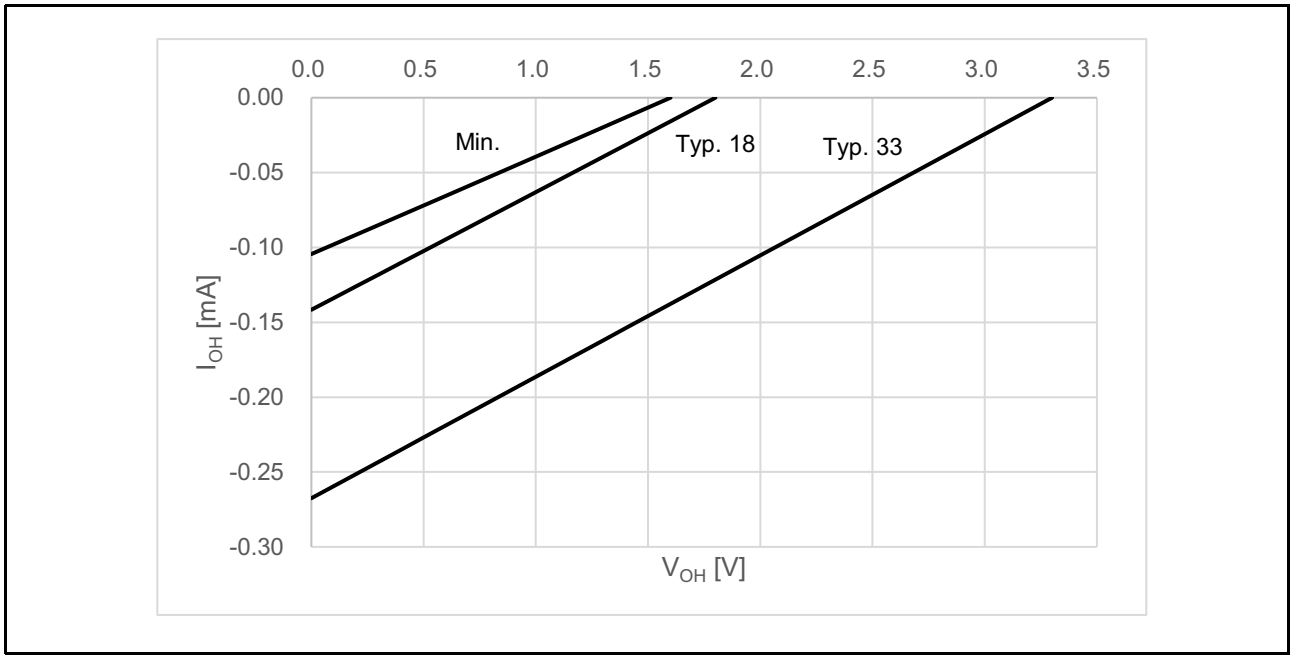


Figure 6.2 V_{OH} vs. I_{OH} Characteristics (Low Driving Ability)

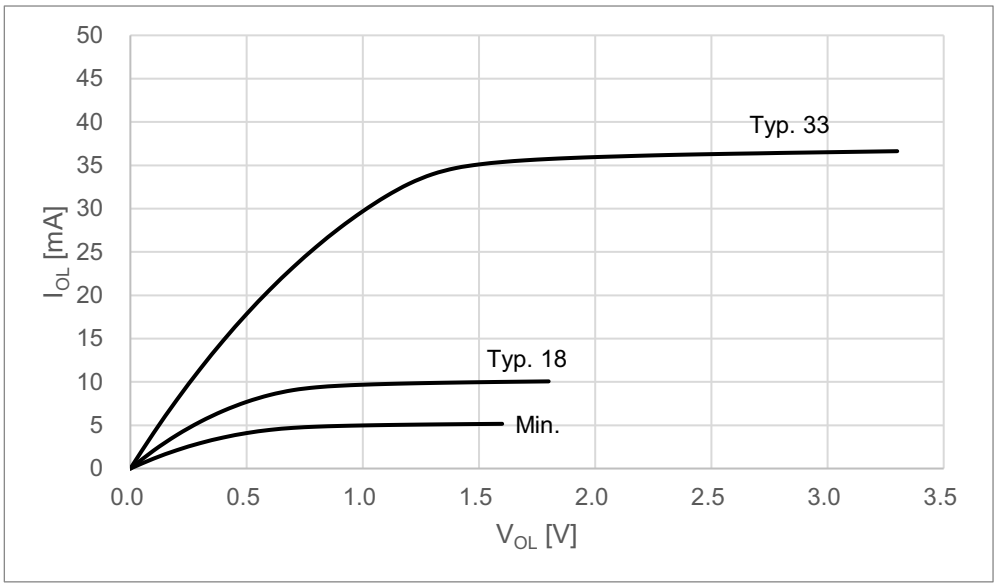


Figure 6.3 V_{OL} vs. I_{OL} Characteristics (Middle Driving Ability)

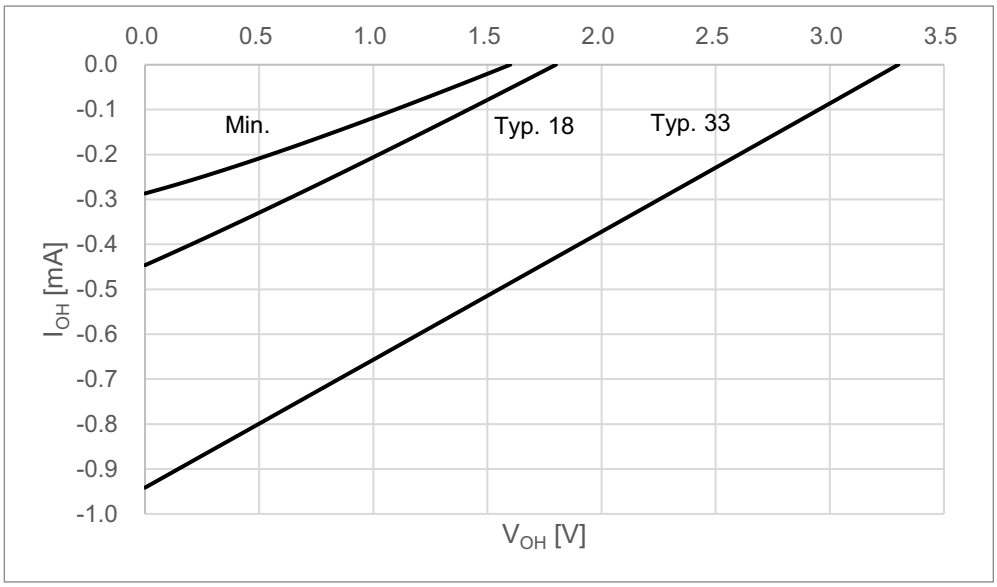


Figure 6.4 V_{OH} vs. I_{OH} Characteristics (Middle Driving Ability)

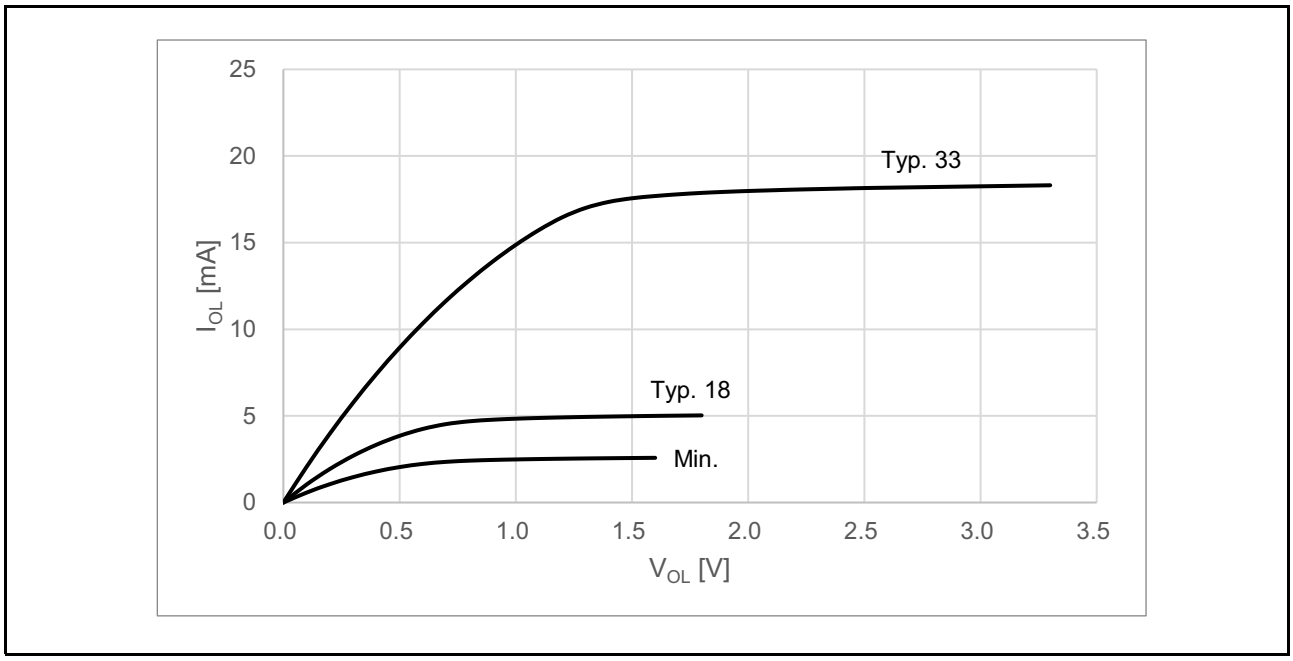


Figure 6.5 V_{OL} vs. I_{OL} Characteristics (Standard Driving Ability)

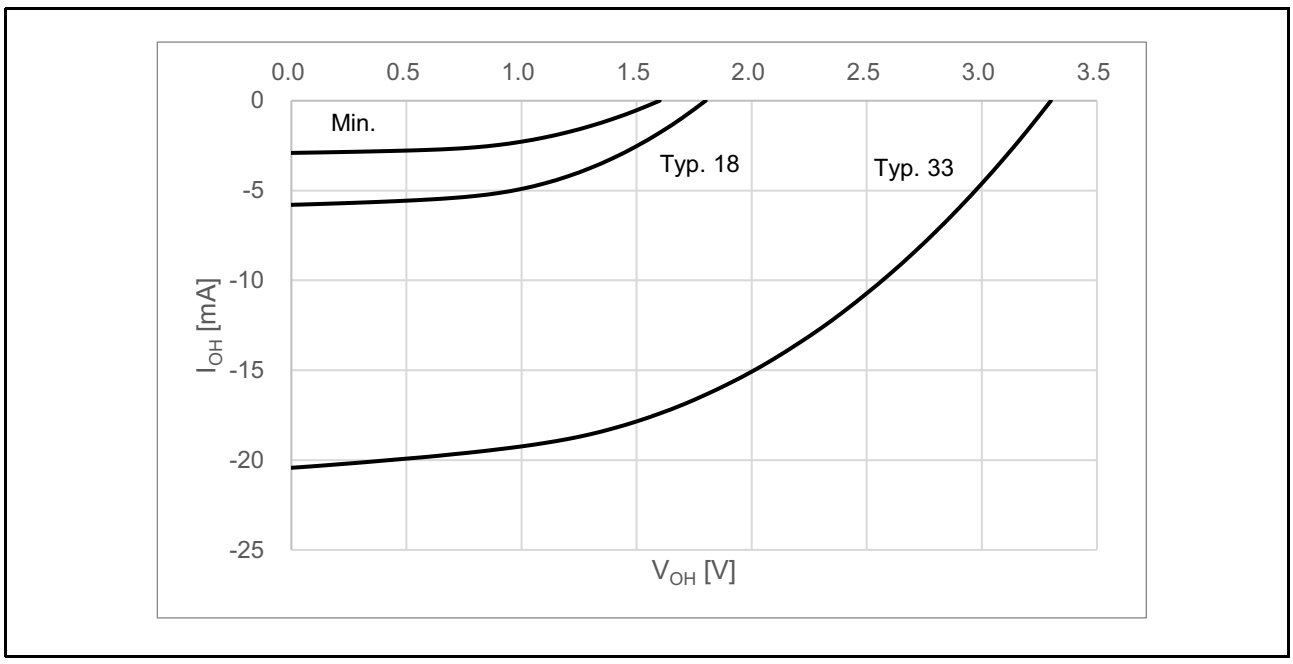


Figure 6.6 V_{OH} vs. I_{OH} Characteristics (Standard Driving Ability)

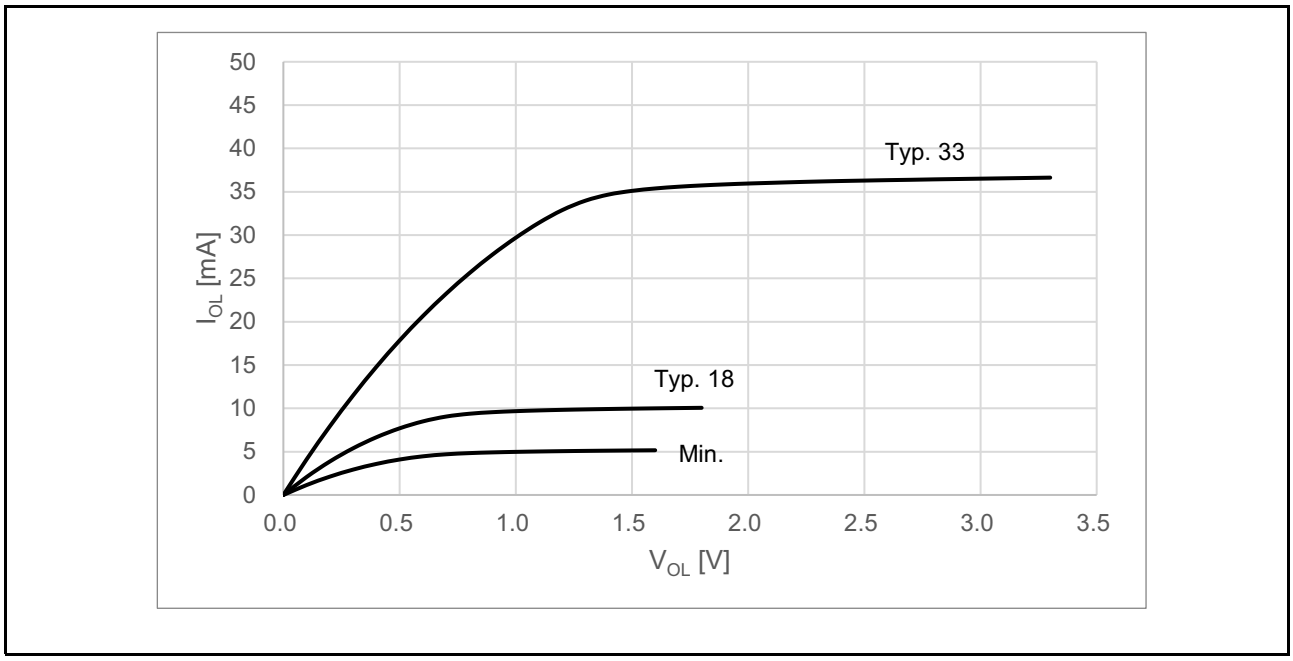


Figure 6.7 V_{OL} vs. I_{OL} Characteristics (High Driving Ability)

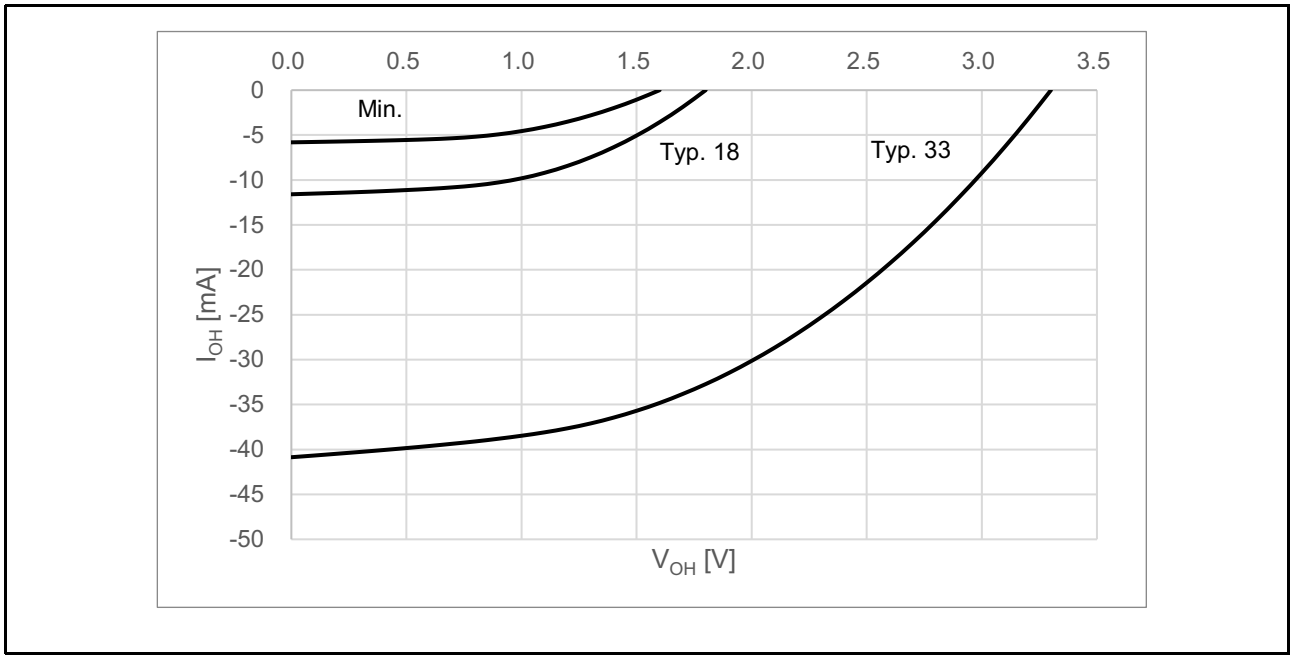


Figure 6.8 V_{OH} vs. I_{OH} Characteristics (High Driving Ability)

6.2.3 Output Characteristics of I/O Pins (V_{OL}) (2)

Table 6.6 Output Characteristics of I/O Pins (V_{OL})
Conditions: VCC = 3.0 to 3.6 V

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output low-level voltage	RIIC	V_{OL}	—	—	0.4	V	I_{OL} = 3 mA
			—	—	0.6		I_{OL} = 6 mA

6.2.4 Pull-up and Pull-down Resistors

Table 6.7 Pull-up and Pull-down Resistors

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Pull-up resistor	I_P	120	200	—	kΩ	VCC = 2.5 V
Pull-down resistor	I_P	120	200	—		VCC = 2.5 V

6.2.5 Pin Capacitance

Table 6.8 Pin Capacitance

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RIIC-related pins	P701, P700	C_{in}	—	—	8	pF	—
EXTAL, XTAL	P412, P413						
All other pins			—	—	16		

Note: For details, see Table 1.4, Pin Functions in section 1, Overview.

6.2.6 Operating Current and Standby Current

Table 6.9 Operating Current and Standby Current (1/6)
Maximum test conditions: VCC = AVCC0 = VREFH0 = 3.6 V, $T_a = T_{opr} = 85°C$
Typical test conditions: VCC = AVCC0 = VREFH0 = 3.3 V, $T_a = T_{opr} = 25°C$
Condition: The FLFSTP bit in the function stop control register is set to 0 (stopping the flash memory function).

Power Supply Mode	Power Control Mode and Low Power Consumption Mode			Specified Operating Frequency	Clock Source	Typ.	Max.	unit
All power supply mode (ALLPWON) The code is executed from within the flash memory.	BOOST	Maximum operation*1		ICLK/PCLKB = 64/32 MHz	HOCO	—	18	mA
				ICLK/PCLKB = 32/16 MHz	HOCO	—	11*3	
		while(1) operation (peripheral clock signal supplied)		ICLK/PCLKB = 64/32 MHz	MOSC + PLL	7.4	—	
				ICLK/PCLKB = 32/16 MHz	MOSC	4.1	—	
				ICLK/PCLKB = 64/32 MHz	HOCO	8.2	—	
				ICLK/PCLKB = 32/16 MHz		4.4	—	
		CoreMark (peripheral clock signal stopped*2)		ICLK/PCLKB = 64/1 MHz	HOCO	3.5	—	
				ICLK/PCLKB = 32/0.5 MHz	HOCO	2.0	—	
		while(1) operation (peripheral clock signal stopped*2)		ICLK/PCLKB = 64/1 MHz	HOCO	3.0	—	
				ICLK/PCLKB = 32/0.5 MHz	HOCO	1.7	—	
		Sleep mode (peripheral clock signal stopped*2)		ICLK/PCLKB = 64/1 MHz	HOCO	1.2	—	
				ICLK/PCLKB = 32/0.5 MHz	HOCO	1.0	—	
		Increases with background operation (BGO)	During programming			0.24	—	
			During erasure			0.23	—	
	NORMAL	High-Speed mode	Maximum operation*1	ICLK/PCLKB = 32/32 MHz	MOSC	—	10	mA
				ICLK/PCLKB = 16/16 MHz		—	8.0*3	
			while(1) operation (peripheral clock signal supplied)	ICLK/PCLKB = 32/32 MHz	MOSC	3.9	9.0	
				ICLK/PCLKB = 16/16 MHz		2.0	7.0*3	
				ICLK/PCLKB = 32/32 MHz	HOCO	4.3	9.0	
				ICLK/PCLKB = 16/16 MHz		2.4	7.0*3	
			CoreMark (peripheral clock signal stopped*2)	ICLK/PCLKB = 32/0.5 MHz	MOSC	1.5	—	
				ICLK/PCLKB = 16/0.25 MHz		0.83	—	
			while(1) operation (peripheral clock signal stopped*2)	ICLK/PCLKB = 32/0.5 MHz	MOSC	1.1	6.0	
				ICLK/PCLKB = 16/0.25 MHz		0.65	—	
			Sleep mode (peripheral clock signal stopped*2)	ICLK/PCLKB = 32/0.5 MHz		0.64	—	
				ICLK/PCLKB = 16/0.25 MHz		0.41	—	
			Increases with background operation (BGO) during programming			0.23	—	
			Increases with background operation (BGO) during erasure			0.15	—	

Table 6.9 Operating Current and Standby Current (2/6)
Maximum test conditions: VCC = AVCC0 = VREFH0 = 3.6 V, $T_a = T_{opr}$ = 85°C
Typical test conditions: VCC = AVCC0 = VREFH0 = 3.3 V, $T_a = T_{opr}$ = 25°C
Condition: The FLFSTP bit in the function stop control register is set to 0 (stopping the flash memory function).

Power Supply Mode	Power Control Mode and Low Power Consumption Mode			Specified Operating Frequency	Clock Source	Typ.	Max.	unit
All power supply mode (ALLPWON) The code is executed from within the flash memory.	NORMAL	Low-Speed mode	Maximum operation*1	ICLK/PCLKB = 2/2 MHz	MOSC	—	5.0	mA
				ICLK/PCLKB = 1/1 MHz		—	5.0*3	
			while(1) operation (peripheral clock signal supplied)	ICLK/PCLKB = 2/2 MHz	MOSC	0.36	5.0*3	
				ICLK/PCLKB = 1/1 MHz		0.24	—	
				ICLK/PCLKB = 2/2 MHz	MOCO	0.36	—	
				ICLK/PCLKB = 1/1 MHz		0.24	—	
			CoreMark (peripheral clock signal stopped*2)	ICLK/PCLKB = 2000/ 31.25 kHz	MOSC	0.20	—	
				ICLK/PCLKB = 1000/ 31.25 kHz		0.15	—	
			while(1) operation (peripheral clock signal stopped*2)	ICLK/PCLKB = 2000/ 31.25 kHz		0.18	—	
				ICLK/PCLKB = 1000/ 31.25 kHz		0.15	—	
			Sleep mode (peripheral clock signal stopped*2)	ICLK/PCLKB = 2000/ 31.25 kHz		0.15	—	
				ICLK/PCLKB = 1000/ 31.25 kHz		0.13	—	
		Subosc-Speed mode	while(1) operation (peripheral clock signal supplied)	ICLK/PCLKB = 32.7/ 32.7 kHz	LOCO	93	4700 *3	µA
				ICLK/PCLKB = 32.7/ 0.51 kHz		92	—	
			while(1) operation (peripheral clock signal stopped*2)	ICLK/PCLKB = 32.7/ 0.51 kHz		91	—	
			Sleep mode (peripheral clock signal stopped*2)	ICLK/PCLKB = 32.7/ 0.51 kHz		90	—	
	VBB	Maximum operation*1		ICLK/PCLKB = 32.7/ 32.7 kHz	LOCO	—	200*3	µA
		while(1) operation (peripheral clock signal supplied)		ICLK/PCLKB = 32.7/ 32.7 kHz		38	—	
		Sleep mode (peripheral clock signal stopped*2)		ICLK/PCLKB = 32.7/ 0.51 kHz		34	—	
		while(1) operation (peripheral clock signal supplied)		ICLK/PCLKB = 32.768/ 32.768 kHz	SOSC (standard CL)	38	—	
		Sleep mode (peripheral clock signal stopped*2)		ICLK/PCLKB = 32.768/ 0.512 kHz		34	—	
		while(1) operation (peripheral clock signal supplied)		ICLK/PCLKB = 32.768/ 32.768 kHz	SOSC (low CL)	37	—	
		Sleep mode (peripheral clock signal stopped*2)		ICLK/PCLKB = 32.768/ 0.512 kHz		33	—	

Table 6.9 Operating Current and Standby Current (3/6)
Maximum test conditions: VCC = AVCC0 = VREFH0 = 3.6 V, $T_a = T_{opr} = 85°C$
Typical test conditions: VCC = AVCC0 = VREFH0 = 3.3 V, $T_a = T_{opr} = 25°C$
Condition: The FLFSTP bit in the function stop control register is set to 0 (stopping the flash memory function).

Power Supply Mode	Power Control Mode and Low Power Consumption Mode			Specified Operating Frequency	Clock Source	Typ.	Max.	unit
Flash excluded power supply mode (EXFPWON) The code is executed from SRAM.	NORMAL	High-Speed mode	Maximum operation*1	ICLK/PCLKB = 32/32 MHz	MOSC	—	9.8*3	mA
				ICLK/PCLKB = 16/16 MHz		—	7.8*3	
			while(1) operation (peripheral clock signal supplied)	ICLK/PCLKB = 32/32 MHz		3.9	—	
				ICLK/PCLKB = 16/16 MHz		2.0	—	
				ICLK/PCLKB = 32/32 MHz	HOCO	4.3	—	
				ICLK/PCLKB = 16/16 MHz		2.4	—	
			while(1) operation (peripheral clock signal stopped*2)	ICLK/PCLKB = 32/0.5 MHz	MOSC	1.1	—	
				ICLK/PCLKB = 16/0.25 MHz		0.61	—	
			Sleep mode (peripheral clock signal stopped*2)	ICLK/PCLKB = 32/0.5 MHz	MOSC	0.59	—	
				ICLK/PCLKB = 16/0.25 MHz		0.36	—	
		Low-Speed mode	Maximum operation*1	ICLK/PCLKB = 2/2 MHz	MOSC	—	4.8*3	
				ICLK/PCLKB = 1/1 MHz		—	4.8*3	
			while(1) operation (peripheral clock signal supplied)	ICLK/PCLKB = 2/2 MHz	MOSC	0.29	—	
				ICLK/PCLKB = 1/1 MHz		0.18	—	
				ICLK/PCLKB = 2/2 MHz	MOCO	0.29	—	
				ICLK/PCLKB = 1/1 MHz		0.18	—	
			while(1) operation (peripheral clock signal stopped*2)	ICLK/PCLKB = 2000/ 31.25 kHz	MOSC	0.13	—	
				ICLK/PCLKB = 1000/ 31.25 kHz		0.10	—	
			Sleep mode (peripheral clock signal stopped*2)	ICLK/PCLKB = 2000/ 31.25 kHz		0.09	—	
				ICLK/PCLKB = 1000/ 31.25 kHz		0.08	—	
		Subosc-Speed mode	while(1) operation (peripheral clock signal supplied)	ICLK/PCLKB = 32.7/ 32.7 kHz	LOCO	52	4500 *3	µA
				ICLK/PCLKB = 32.7/ 0.51 kHz		51	—	
			while(1) operation (peripheral clock signal stopped*2)	ICLK/PCLKB = 32.7/ 0.51 kHz		50	—	
			Sleep mode (peripheral clock signal stopped*2)	ICLK/PCLKB = 32.7/ 0.51 kHz		49	—	

Table 6.9 Operating Current and Standby Current (4/6)
Maximum test conditions: VCC = AVCC0 = VREFH0 = 3.6 V, $T_a = T_{opr} = 85°C$
Typical test conditions: VCC = AVCC0 = VREFH0 = 3.3 V, $T_a = T_{opr} = 25°C$
Condition: The FLFSTP bit in the function stop control register is set to 0 (stopping the flash memory function).

Power Supply Mode	Power Control Mode and Low Power Consumption Mode			Specified Operating Frequency	Clock Source	Typ.	Max.	unit
Flash excluded power supply mode (EXFPWON) The code is executed from SRAM.	NORMAL	Software standby mode*4	VCC = 3.3 V		LOCO	29	—	µA
			VCC = 1.8 V			29	—	
			VCC = 3.3 V		SOSC (standard CL)	29	—	
			VCC = 1.8 V			29	—	
			VCC = 3.3 V		SOSC (low CL)	28	—	
			VCC = 1.8 V			28	—	
	VBB	Maximum operation*1		ICLK/PCLKB = 32.7/32.7 kHz	LOCO	—	30*3	
		while(1) operation (peripheral clock signal supplied)		ICLK/PCLKB = 32.7/32.7 kHz		6.8	—	
		Sleep mode (peripheral clock signal stopped*2)		ICLK/PCLKB = 32.7/0.51 kHz		3.1	—	
		Software standby mode*4	VCC = 3.3 V/3.6 V			2.1	25*3	
			VCC = 1.8 V			1.9	—	
		while(1) operation (peripheral clock signal supplied)		ICLK/PCLKB = 32.768/32.768 kHz	SOSC (standard CL)	6.5	—	
		Sleep mode (peripheral clock signal stopped*2)		ICLK/PCLKB = 32.768/0.512 kHz		2.9	—	
		Software standby mode*4	VCC = 3.3 V			2.0	—	
			VCC = 1.8 V			1.9	—	
		while(1) operation (peripheral clock signal supplied)		ICLK/PCLKB = 32.768/32.768 kHz	SOSC (low CL)	5.8	—	
		Sleep mode (peripheral clock signal stopped*2)		ICLK/PCLKB = 32.768/0.512 kHz		2.2	—	
		Software standby mode*4	VCC = 3.3 V			1.3	—	
			VCC = 1.8 V			1.2	—	
Minimum power supply mode (MINPWON) The code is executed from SRAM	NORMAL	High-Speed mode	Maximum operation*1	ICLK/PCLKB = 32/32 MHz	MOSC	—	7.0*3	mA
				ICLK/PCLKB = 16/16 MHz		—	5.5*3	
			while(1) operation (peripheral clock signal stopped*2)	ICLK/PCLKB = 32/0.5 MHz	MOSC	1.1	4.6*3	
				ICLK/PCLKB = 16/0.5 MHz		0.8	—	
			Sleep mode (peripheral clock signal stopped*2)	ICLK/PCLKB = 32/0.5 MHz	MOSC	0.58	—	
				ICLK/PCLKB = 16/0.5 MHz		0.42	—	

Table 6.9 Operating Current and Standby Current (5/6)
Maximum test conditions: VCC = AVCC0 = VREFH0 = 3.6 V, $T_a = T_{opr} = 85°C$
Typical test conditions: VCC = AVCC0 = VREFH0 = 3.3 V, $T_a = T_{opr} = 25°C$
Condition: The FLFSTP bit in the function stop control register is set to 0 (stopping the flash memory function).

Power Supply Mode	Power Control Mode and Low Power Consumption Mode			Specified Operating Frequency	Clock Source	Typ.	Max.	unit
Minimum power supply mode (MINPWON) The code is executed from SRAM	NORMAL	Low-Speed mode	Maximum operation*1	ICLK/PCLKB = 2/2 MHz	MOSC	—	3700 *3	µA
				ICLK/PCLKB = 1/1 MHz		—	3700 *3	
			while(1) operation (peripheral clock signal stopped*2)	ICLK/PCLKB = 2000/ 31.25 kHz	MOSC	110	—	
				ICLK/PCLKB = 1000/ 31.25 kHz		80	—	
				ICLK/PCLKB = 2000/ 31.25 kHz	MOCO	105	—	
				ICLK/PCLKB = 1000/ 31.25 kHz		75	—	
			Sleep mode (peripheral clock signal stopped*2)	ICLK/PCLKB = 2000/ 31.25 kHz	MOCO	70	—	
				ICLK/PCLKB = 1000/ 31.25 kHz		60	—	
		Subosc-Speed mode	while(1) operation (peripheral clock signal stopped*2)	ICLK/PCLKB = 32.7/ 32.7 kHz	LOCO	40	3500 *3	µA
				ICLK/PCLKB = 32.7/ 0.51 kHz		40	—	
			Sleep mode (peripheral clock signal stopped*2)	ICLK/PCLKB = 32.7/ 32.7 kHz		39	—	
				ICLK/PCLKB = 32.7/ 0.51 kHz		39	—	
		Software standby mode*4	VCC = 3.3 V		LOCO	20	—	µA
			VCC = 1.8 V			19	—	
			VCC = 3.3 V		SOSC (standard CL)	20	—	
			VCC = 1.8 V			20	—	
			VCC = 3.3 V		SOSC (low CL)	19	—	
			VCC = 1.8 V			19	—	
	VBB	while(1) operation (peripheral clock signal supplied)		ICLK/PCLKB = 32.768/ 32.768 kHz	SOSC (standard CL)	3.3	22*3	µA
		Sleep mode (peripheral clock signal stopped*2)		ICLK/PCLKB = 32.768/ 0.512 kHz		1.8	—	
		Software standby mode*4	VCC = 3.3 V			1.4	—	
			VCC = 1.8 V			1.2	—	
		while(1) operation (peripheral clock signal supplied)		ICLK/PCLKB = 32.7/ 32.7 kHz	LOCO	3.3	15*3	µA
		Sleep mode (peripheral clock signal stopped*2)		ICLK/PCLKB = 32.7/ 0.51 kHz		1.8	14*3	
		Software standby mode*4	VCC = 3.3 V (typ.)/3.6 V (max.)			1.4	12	
			VCC = 1.8 V			1.2	10*3	
		while(1) operation (peripheral clock signal supplied)		ICLK/PCLKB = 32.768/ 32.768 kHz	SOSC (low CL)	2.6	—	µA
		Sleep mode (peripheral clock signal stopped*2)		ICLK/PCLKB = 32.768/ 0.512 kHz		1.1	—	
		Software standby mode*4	VCC = 3.3 V			0.7	—	
			VCC = 1.8 V			0.5	—	
Minimum power supply mode (MINPWON) The code is executed from SRAM	VBB	Software standby mode Increases when peripheral modules are in use (independent of VCC)	Increase for using the IWDT (OFS0.IWDTSTRT = 0)			81	—	nA
			Increase for using the AGT (AGTCR.TSTART = 1)			43	—	
			Increase for each 32 Kbytes of SRAM in use (set by the RAMSDCR register)			12	—	

Table 6.9 Operating Current and Standby Current (6/6)
Maximum test conditions: VCC = AVCC0 = VREFH0 = 3.6 V, $T_a = T_{opr} = 85°C$
Typical test conditions: VCC = AVCC0 = VREFH0 = 3.3 V, $T_a = T_{opr} = 25°C$
Condition: The FLFSTP bit in the function stop control register is set to 0 (stopping the flash memory function).

Power Supply Mode	Power Control Mode and Low Power Consumption Mode	Specified Operating Frequency	Clock Source	Typ.	Max.	unit
Deep software standby mode	VCC = 3.3 V (typ.)/3.6 V (max.)	—	—	140	2000 *3	nA
	VCC = 1.8 V	—	—	120	500*3	
	Increase for using the SOSC (VCC = 3.3 V)	—	SOSC (low CL)	160	—	
	Increase for using the SOSC (VCC = 1.8 V)	—		100	—	
Increases when peripheral modules are in use in standby mode (independent of VCC)	Increase for using the LVD0 (OFS1.LVDAS = 0)			48	—	nA
	Increase for using the LVD1 (LVCMPCR.LVD1E = 1)			66	—	
	Increase for using the LVDBAT (LVCMPCR.LVDBATE = 1)			66	—	
	Increase for using the CCC (CADJUSCEN = 1 and ADJUSTEN = 1)			35	—	

Note 1. The value for current in a “Maximum operation” row is for a case where the DMAC is handling transfer in every cycle and the CPU is repeatedly executing a multiply instruction while all modules are released from the module-stop state. The value does not include the current during background operation (BGO) and the supply of current for the pins.
Note 2. The value for current in a row with a label that includes “peripheral clock signal stopped” is for a case where the peripheral circuits have been placed in the module-stop state following the settings for frequency-division of ICLK and PCLKB.
Note 3. We do not inspect this value before shipment. The values presented in this manual are only for reference.
Note 4. The supply of the clock signals is stopped in this mode regardless of the operating frequency settings.

Table 6.10 Analog Operating Current (AVCC0) and Standby Current
Maximum test conditions: VCC = AVCC0 = 3.6 V, $T_a = T_{opr} = 85°C$
Typical test conditions: VCC = AVCC0 = VREFH0 = 3.3 V, $T_a = T_{opr} = 25°C$ (when the VREF is not in use)
Typical test conditions: VCC = AVCC0 = 3.3 V, AVTRO = 1.25 V, $T_a = T_{opr} = 25°C$ (when the VREF is in use)

Item	Operating Circuit			Symbol	Typ.	Max.	Unit	Test Conditions
	A/D	Temperature Sensor	VREF					
AVCC0 power supply current	During conversion	During operation	During operation	I_{AVCC0}	81	—	µA	PCLKB = 16 MHz Sampling interval is 1 µs. (ADSSTRn.SST[7:0] = 10h)
		Stopped	During operation		77	—		
		During operation	Stopped		69	—		
		Stopped	Stopped		53	—		
		Stopped	Stopped		0.19	—		PCLKB = 32.768 kHz Sampling interval is 61 µs. (ADSSTRn.SST[7:0] = 02h)
	Waiting for conversion	Stopped	Stopped		22	—	nA	PCLKB = 16 MHz*1
	On standby				22	1900		Clock supply is stopped.
Reference power supply current	During conversion	Stopped	Stopped	I_{REFH0}	18	—	µA	PCLKB = 16 MHz
					0.08	—		PCLKB = 32.768 kHz
	Waiting for conversion	Stopped	Stopped		22	—	nA	PCLKB = 16 MHz*1
	On standby				22	—		Clock supply is stopped.

Note 1. This indicates that the clock signal is being supplied to the A/D converter but A/D conversion is not in progress.

Table 6.11 BLE Operating Current and Standby Current
Conditions: VCC = AVCC0 = VCC_RF = AVCC_RF = 3.3 V, VSS = AVSS0 = VSS_RF = 0 V, T_a = +25°C

Item	Symbol	Typ.		Unit	Test Conditions
		Transmit output power			
		0 dBm	4 dBm		
BLE operating current (when the DC-to-DC converter is selected)	Idd_tx	4.3	8.7	mA	Transmit mode, 2 Mbps
					Transmit mode, 1 Mbps
		4.5	8.7		Transmit mode, 500 kbps
					Transmit mode, 125 kbps
	Idd_rx	3.0	3.5	mA	Receive mode, 2 Mbps Prf = –67 dBm
		3.0	3.4		Receive mode, 1 Mbps Prf = –67 dBm
		3.2	3.5		Receive mode, 500 kbps Prf = –72 dBm
		3.3	3.5		Receive mode, 125 kbps Prf = –79 dBm
	Idd_idle	0.5		mA	Idle mode
	Idd_slp	1.5		µA	Deep sleep mode
	Idd_down	0.1		µA	Power down mode
BLE operating current (when the linear regulator is selected)	Idd_tx	10.2	18.1	mA	Transmit mode, 2 Mbps
					Transmit mode, 1 Mbps
					Transmit mode, 500 kbps
					Transmit mode, 125 kbps
	Idd_rx	6.9		mA	Receive mode, 2 Mbps Prf = –67 dBm
		6.9			Receive mode, 1 Mbps Prf = –67 dBm
		6.9			Receive mode, 500 kbps Prf = –72 dBm
		7.1			Receive mode, 125 kbps Prf = –79 dBm
	Idd_idle	0.7		mA	Idle mode
	Idd_slp	1.5		µA	Deep sleep mode
	Idd_down	0.1		µA	Power down mode

Table 6.12 IOVCC Waiting Current
Maximum test conditions: VCC = IOVCCn = 3.6 V, $T_a = T_{opr}$ = 85°C
Typical test conditions: VCC = IOVCCn = 3.3 V, $T_a = T_{opr}$ = 25°C

Item	Symbol	Typ.	Max.	Unit	Test Conditions
IOVCC0 waiting current	$I_{IOVCC0ST}$	8.6	—	nA	—
IOVCC1 waiting current	$I_{IOVCC1ST}$	16	—		—
IOVCC2 waiting current	$I_{IOVCC2ST}$	9.2	—		—
IOVCC3 waiting current	$I_{IOVCC3ST}$	21	—		—
IOVCC0 to IOVCC3 waiting current (total)	$I_{IOVCCST}$	—	900		

6.2.7 Gradients of VCC Rising and Falling

Table 6.13 Characteristics for Gradients of VCC Rising and Falling

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Range of gradients for VCC rising at the time power is supplied	SrVCC	0.02	—	20	ms/V	—
Allowable range of fluctuations in the gradients for the voltage rising and falling	dt/dVCC	2	—	20	ms/V	—

6.2.8 On-chip Linear Regulator Characteristics

Table 6.14 On-chip Linear Regulator Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LDO startup time	t_{LDO}	3000	—	—	µs	Figure 6.9
LDO stabilization time	t_{LDOWT}	300	—	—	µs	Figure 6.9

Note: To ensure stable operation of the LSI chip, avoid operations that draw large amounts of current during the LDO stabilization time and the LDO stabilization period after no externally applied voltage is being supplied.

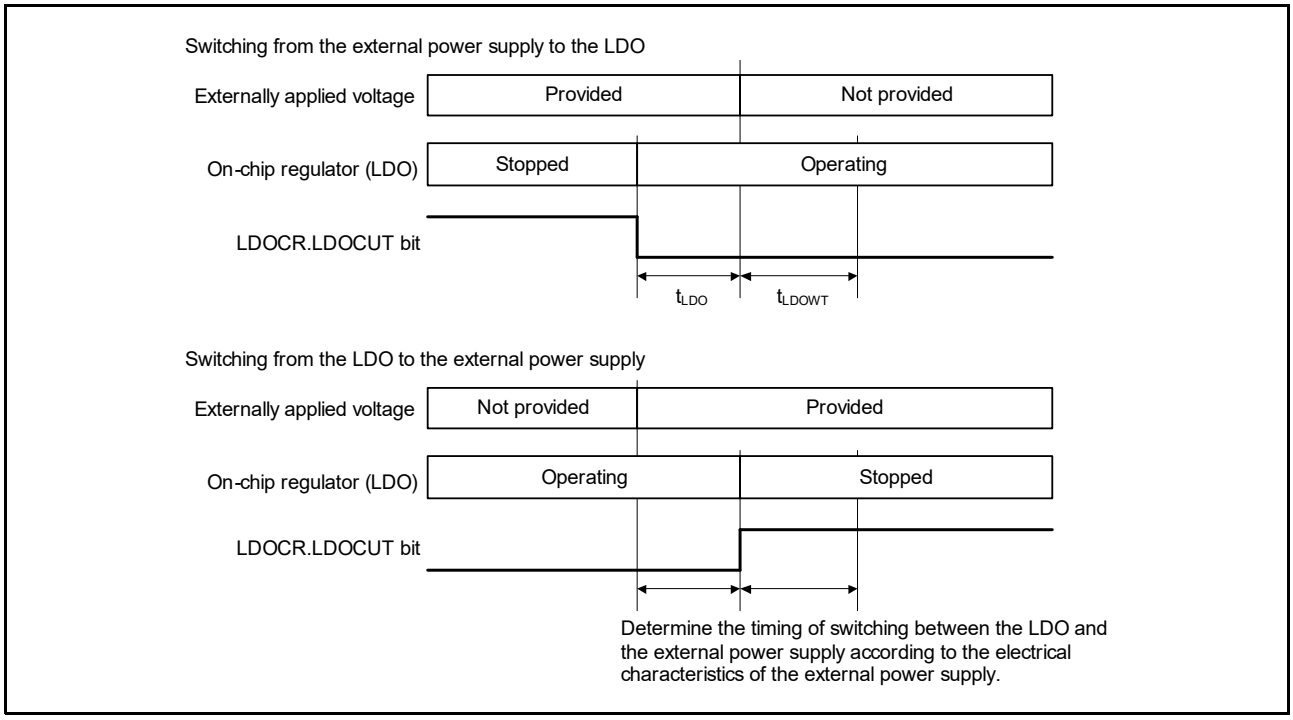


Figure 6.9 Timing of Switching between the External Power Supply and the LDO

6.3 AC Characteristics

6.3.1 Operating Frequency

Table 6.15 Operating Frequencies in the Various Modes

Power Control Mode		Clock Source	Symbol	Min.	Typ.	Max.	Unit
BOOST		System clock (ICLK)	f	—	—	64	MHz
		Peripheral module clock A (PCLKA)		—	—	64	
		Peripheral module clock B (PCLKB)		—	—	32	
NORMAL	High-speed	System clock (ICLK)		—	—	32	
		Peripheral module clock A (PCLKA)		—	—	32	
		Peripheral module clock B (PCLKB)		—	—	32	
	Low-speed	System clock (ICLK)		—	*1	2.3	
		Peripheral module clock A (PCLKA)		—	*1	2.3	
		Peripheral module clock B (PCLKB)		—	*1	2.3	
	Subosc-speed	System clock (ICLK)		—	*2	37.6	kHz
		Peripheral module clock A (PCLKA)		—	*2	37.6	
		Peripheral module clock B (PCLKB)		—	*2	37.6	
VBB		System clock (ICLK)		—	*2	37.6	
		Peripheral module clock A (PCLKA)		—	*2	37.6	
		Peripheral module clock B (PCLKB)		—	*2	37.6	

Note: Reading, programming, and erasing the code flash memory requires that operation be within a specific range of frequencies. See Table 48.3 in section 48, Flash Memory in the User's Manual: Hardware.

Note: For the required relationships between the frequencies of clock signals, see the note under Table 9.2 in section 9, Clock Generation Circuit in the User's Manual: Hardware.

Note 1. The value is 2.0 MHz when the MOCO is selected as the clock source and the frequency is not being divided.

Note 2. The value is 32.768 kHz when the sub-clock oscillator is selected as the clock source and the frequency is not being divided.

6.3.2 Clock Timing

Table 6.16 Timing of the Clock Signals other than the Sub-clock Oscillator

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{EXcyc}	35	—	—	ns	Figure 6.10
EXTAL external clock input high pulse width	t_{EXH}	14	—	—	ns	
EXTAL external clock input low pulse width	t_{EXL}	14	—	—	ns	
EXTAL external clock input rising time	t_{EXr}	—	—	3.5	ns	
EXTAL external clock input falling time	t_{EXf}	—	—	3.5	ns	
Main clock oscillator frequency	f_{MAIN}	8	—	32	MHz	—
Waiting time till the main clock oscillation is stable (crystal)*1	$t_{MAINOSCWT}$	—	—	—*1	ms	Figure 6.11
LOCO clock oscillation frequency	f_{LOCO}	27.8	32.7	37.6	kHz	—
Waiting time till the LOCO clock oscillation is stable	t_{LOCOWT}	—	—	130	µs	Figure 6.12
IWDT-dedicated clock oscillation frequency	$f_{IWDTLOCO}$	13.9	16.35	18.8	kHz	—
Bluetooth-dedicated clock oscillation frequency	f_{BLECK}	—	32	—	MHz	—
Bluetooth-dedicated low-speed on-chip oscillator oscillation frequency	$f_{BLELOCO}$	—	32.768	—	kHz	—
MOCO clock oscillation frequency	f_{MOCO}	1.4	2	2.3	MHz	—
Waiting time till the MOCO clock oscillation is stable	t_{MOCOWT}	—	—	16	µs	—
HOCO clock oscillation frequency*3	f_{HOCO24}	23.52	24	24.96	MHz	0°C ≤ T_a ≤ +85°C
	f_{HOCO32}	31.36	32	33.28		
	f_{HOCO48}	47.04	48	49.92		
	f_{HOCO64}	62.72	64	66.56		
	f_{HOCO24}	22.80	24	24.96		–40°C ≤ T_a ≤ 85°C
	f_{HOCO32}	30.40	32	33.28		
	f_{HOCO48}	45.60	48	49.92		
	f_{HOCO64}	60.80	64	66.56		
HOCO clock oscillation stabilization wait time*2	t_{HOCOWT}	—	—	700	µs	—
PLL output clock frequency	f_{PLL}	32	—	64	MHz	PLLCCR.FSEL0 = 1
		32	—	48		PLLCCR.FSEL0 = 0
Waiting time till the PLL output clock oscillation is stable	t_{PLLWT}	—	—	1020	µs	Figure 6.13 Includes the stabilization waiting time for LOCO clock oscillation

Note 1. For setting up the main clock oscillator, we recommend consulting the oscillator manufacturer regarding the results of oscillation evaluation and use the results for the oscillation stabilization time. The value of the MOSCWTCR register should correspond to at least that value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.
Note 2. This is the time period between when HOCOCR.HCSTP is changed to 0 and when OSCSF.HOCOSF is changed to 1.
Note 3. The guaranteed values stated for this item apply to products in packages. Note that these characteristics will deteriorate due to fluctuations in stress when the sample device has been mounted on your system.

Table 6.17 Timing of the Sub-clock Oscillator

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Sub-clock frequency	f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	—	—	—*1	s	Figure 6.14

Note 1. For setting up the sub-clock oscillator, we recommend consulting the oscillator manufacturer regarding the results of oscillation evaluation and use the results for the oscillation stabilization time. After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. We recommend using two times the value of the results of oscillation evaluation by the oscillator manufacturer.

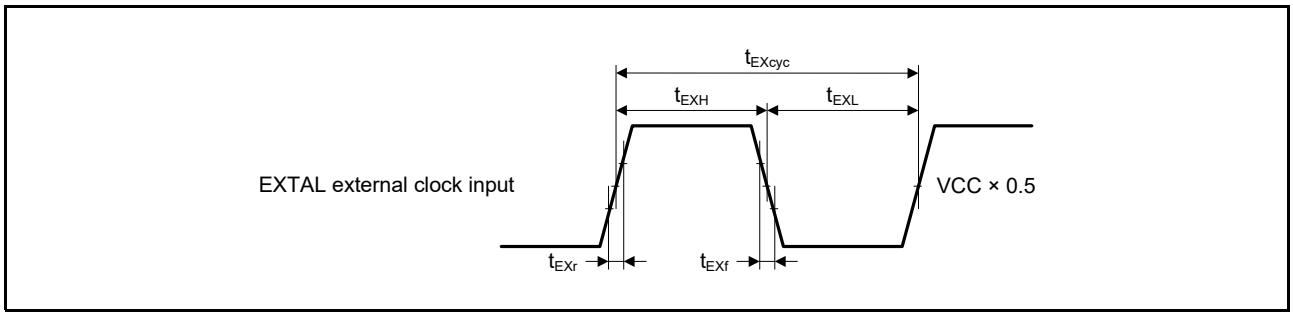


Figure 6.10 EXTAL External Clock Input Timing

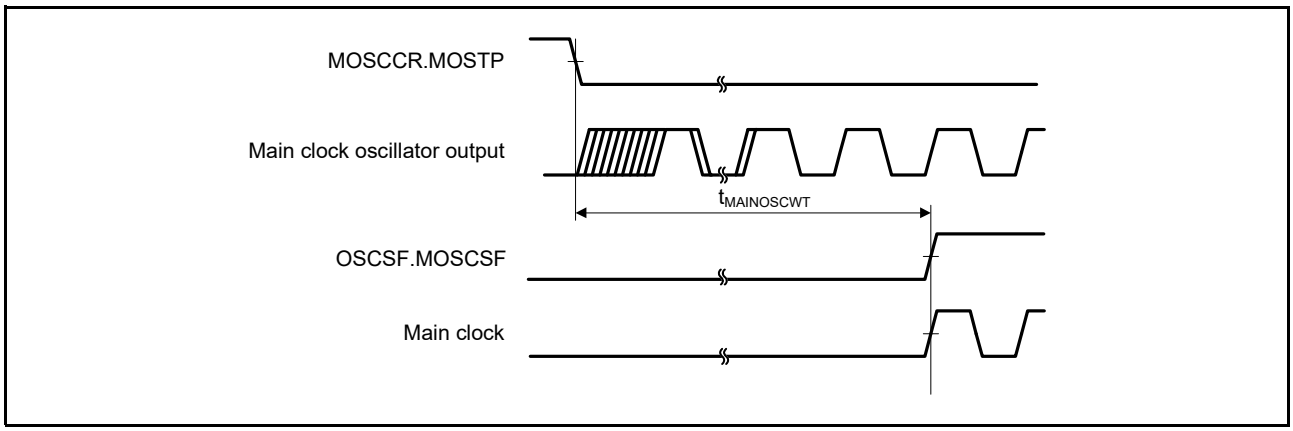


Figure 6.11 Main Clock Oscillation Start Timing

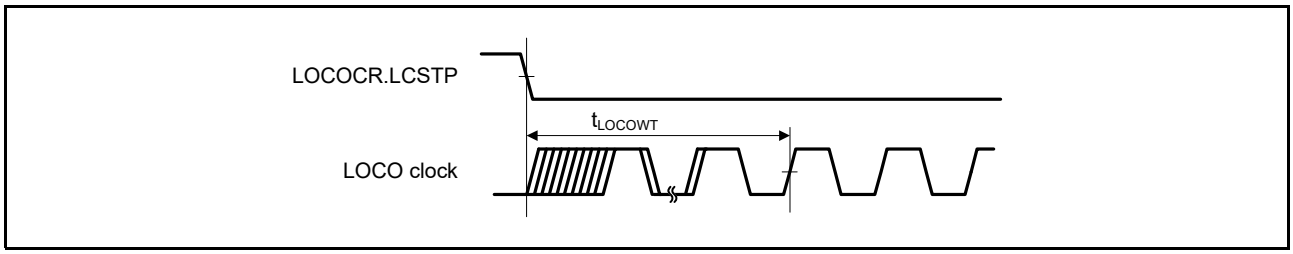


Figure 6.12 LOCO Clock Oscillation Start Timing

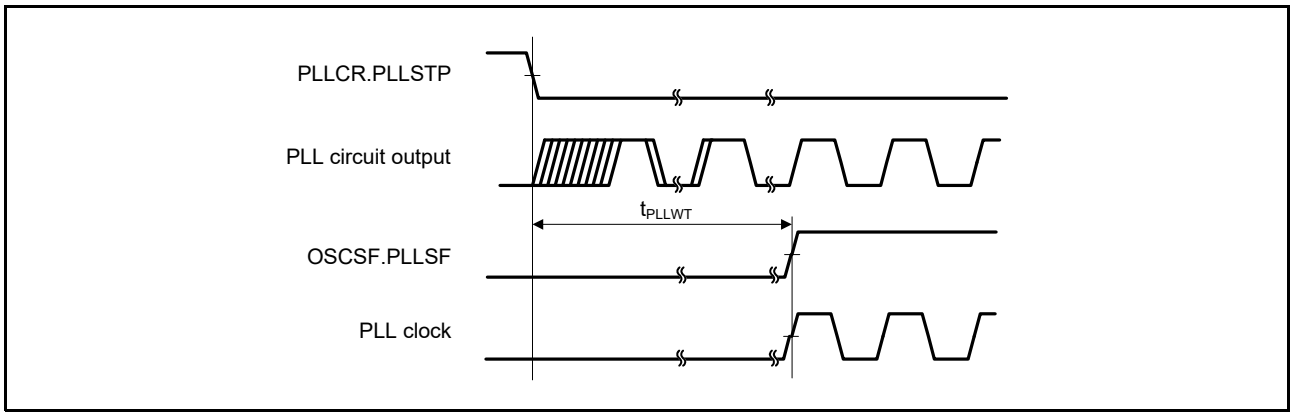


Figure 6.13 PLL Clock Oscillation Start Timing

Note: Start the PLL after the main clock oscillation is stabilized.

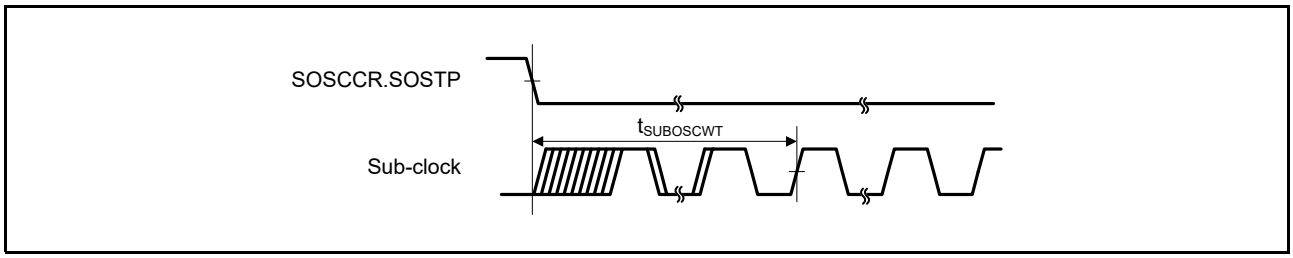


Figure 6.14 Sub-clock Oscillation Start Timing

6.3.3 Reset Timing

Table 6.18 Reset Timing

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on (in the normal startup mode)		t_{RESWP}	44	—	—	ms	Figure 6.15
	Deep software standby mode (in the normal startup mode)		t_{RESWD}	13	—	—	ms	Figure 6.16
	Software standby mode, Subosc-speed mode		t_{RESWS}	7.0	—	—	ms	
	ALLPWON	Operation in boost mode	t_{RESW}	0.9	—	—	ms	
		Operation in normal mode	t_{RESW}	0.6	—	—	ms	
		Operation in low leakage current mode	t_{RESW}	1.6	—	—	ms	
		Transition from boost mode to normal mode in progress	t_{RESW}	0.6	—	—	ms	
		Transition from normal mode to boost mode in progress	t_{RESW}	1.8	—	—	ms	
		Transition from normal mode to low leakage current mode in progress	t_{RESW}	2.1	—	—	ms	
		Transition from low leakage current mode to normal mode in progress	t_{RESW}	1.2	—	—	ms	
	EXFPWON	Operation in normal mode	t_{RESW}	1.9	—	—	ms	
		Operation in low leakage current mode	t_{RESW}	2.0	—	—	ms	
		Transition from normal mode to low leakage current mode in progress	t_{RESW}	2.4	—	—	ms	
		Transition from low leakage current mode to normal mode in progress	t_{RESW}	2.1	—	—	ms	
	MINPWON	Operation in normal mode	t_{RESW}	2.3	—	—	ms	
		Operation in low leakage current mode	t_{RESW}	2.5	—	—	ms	
		Transition from normal mode to low leakage current mode in progress	t_{RESW}	6.1	—	—	ms	
		Transition from low leakage current mode to normal mode in progress	t_{RESW}	2.6	—	—	ms	
	Transition between ALLPWON and EXFPWON modes in normal mode in progress		t_{RESW}	2.5	—	—	ms	
	Transition between EXFPWON and MINPWON modes in normal mode in progress		t_{RESW}	2.0	—	—	ms	
	Transition between ALLPWON and EXFPWON modes in VBB mode in progress		t_{RESW}	3.0	—	—	ms	
	Transition between EXFPWON and MINPWON modes in VBB mode in progress		t_{RESW}	6.5	—	—	ms	
Waiting time after release from the RES# pin reset			t_{RESWT}	—	19	22	ms	Figure 6.15, Figure 6.16

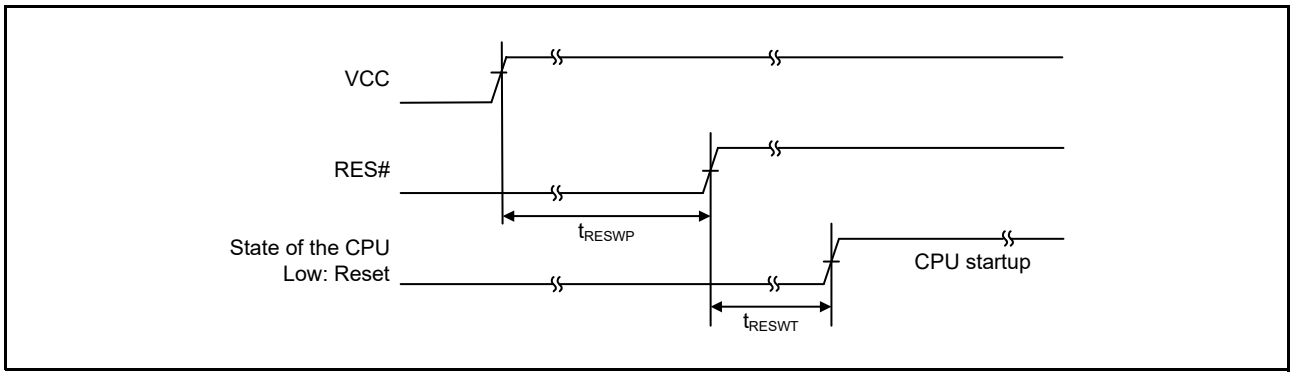


Figure 6.15 Timing of Input through the Reset Pin when Power is Supplied

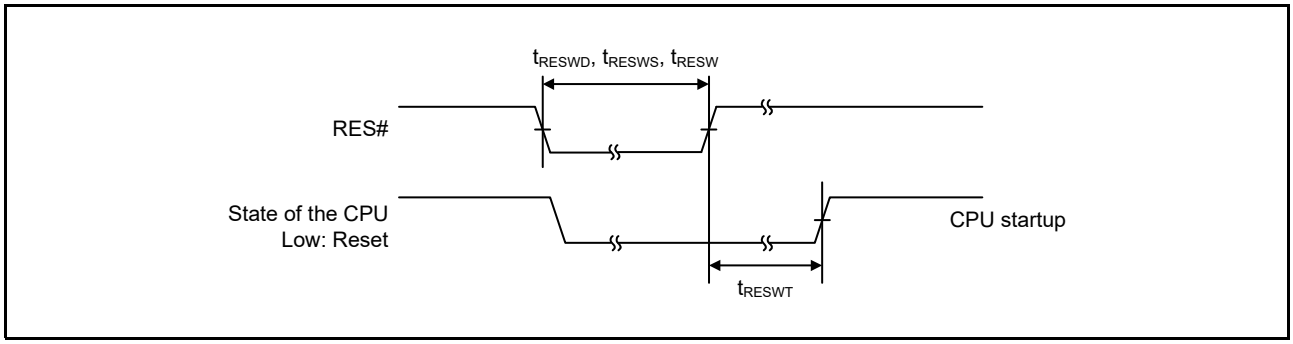


Figure 6.16 Reset Input Timing

6.3.4 Wakeup Timing

Table 6.19 Timing of Return from Low Power Consumption (Standby) Mode

Item	Power Control Mode before and after the Mode Transition	System Clock Source	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Time to return to operating mode (ALLPWON) from software standby (EXFPWON)*1	VBB	SOSC	t_{SBYSC}	—	—	6.0	ms	All oscillators have the same frequency divisor of 1. Measurement was in the ALLPWON power supply mode.
		LOCO	t_{SBYLO}	—	—	6.2	ms	
Time to return to operating mode (EXFPWON) from software standby (EXFPWON)*1	VBB	SOSC	t_{SBYSC}	—	—	1.2	ms	All oscillators have the same frequency divisor of 1. Measurement was in the EXFPWON power supply mode.
		LOCO	t_{SBYLO}	—	—	1.1	ms	
Time to return to operating mode (MINPWON) from software standby (MINPWON)*1	VBB	SOSC	t_{SBYSC}	—	—	1.2	ms	All oscillators have the same frequency divisor of 1. Measurement was in the MINPWON power supply mode.
		LOCO	t_{SBYLO}	—	—	1.1	ms	
Time to return from deep software standby (in normal startup mode)			t_{DSBY}	—	—	9	ms	Figure 6.17
Waiting time following release from deep software standby			t_{DSBYWT}	—	—	22	ms	

Note 1. The system clock source determines the time return takes. If multiple oscillators are started, the time return takes can be calculated from the following expression. Total time for return = time for return of the oscillator that serves as the system source clock + maximum oscillation stabilization time of an oscillator that requires more stabilization time than the system source clock + 2 cycles of LOCO (if LOCO is to operate) + 3 cycles of SOSC (if the sub-clock oscillator is to operate and MSTPCRC.MSTPC0 = 0 (releasing the CAC from the module-stop state)).

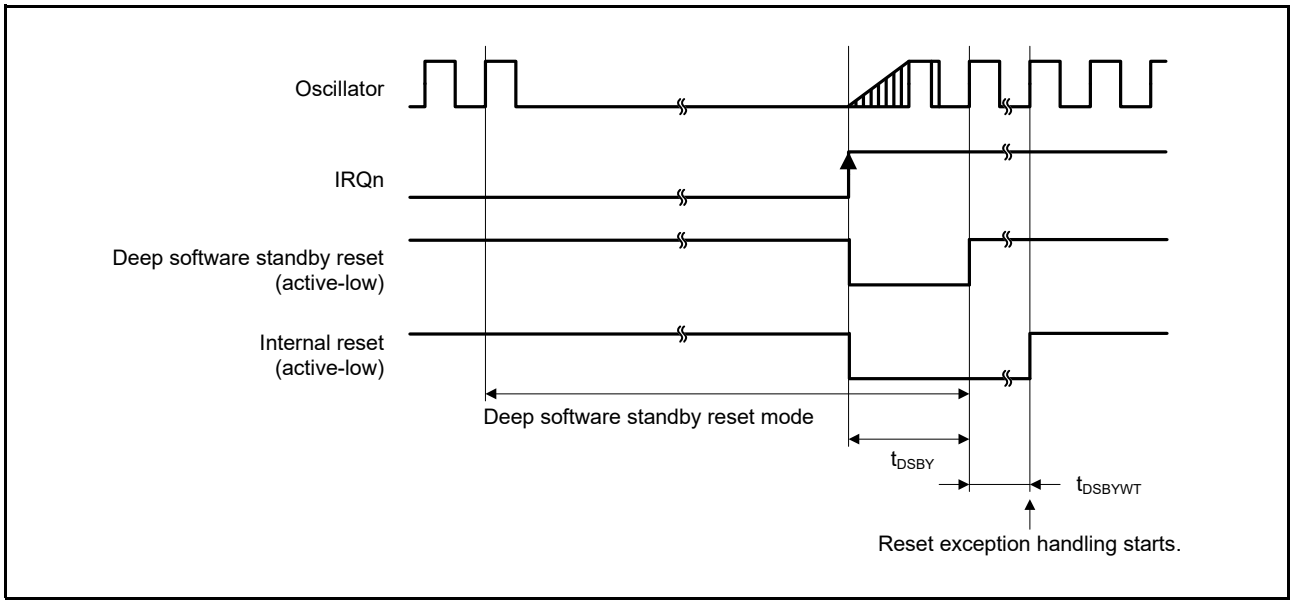


Figure 6.17 Timing of Release from Deep Software Standby

6.3.5 Interrupt Input Timing

Table 6.20 Interrupt Input Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	6000	—	—	ns	Software standby in low leakage current mode
		1000	—	—		Software standby when not in low leakage current mode
		300	—	—		In deep software standby mode
		4	—	—	t_{Pcyc}*1	Other than above
IRQn pulse width	t_{IRQW}	6000	—	—	ns	Software standby in low leakage current mode
		1000	—	—		Software standby when not in low leakage current mode
		300	—	—		In deep software standby mode
		4	—	—	t_{Pcyc}*1	Other than above IRQCRi.IRQMD[1:0] = 00b, 01b
		5	—	—		Other than above IRQCRi.IRQMD[1:0] = 10b
KINT pulse width	t_{KINTW}	6000	—	—	ns	Software standby in low leakage current mode
		1000	—	—		Software standby when not in low leakage current mode
		4	—	—	t_{Pcyc}*1	In deep software standby mode

Note 1. t_{Pcyc} refers to the period of a cycle of PCLKB.

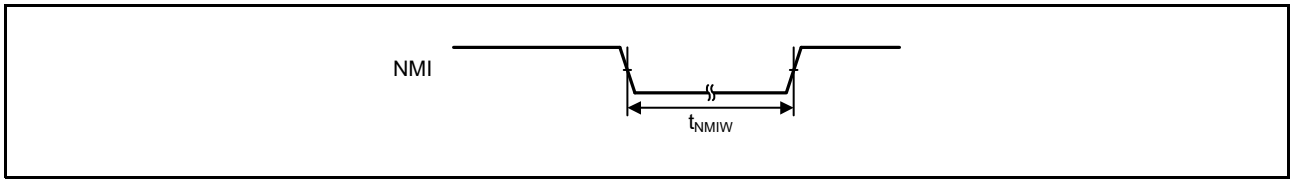


Figure 6.18 NMI Interrupt Input Timing

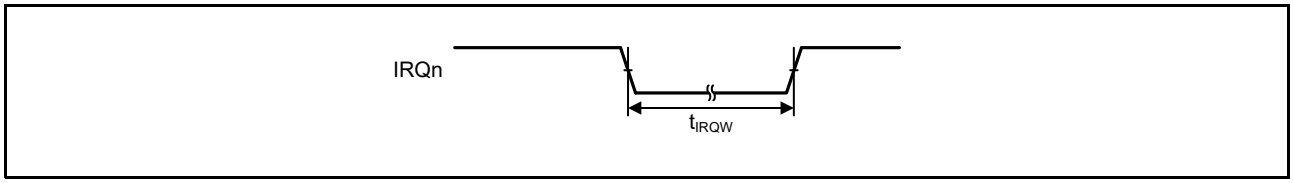


Figure 6.19 IRQn Interrupt Input Timing

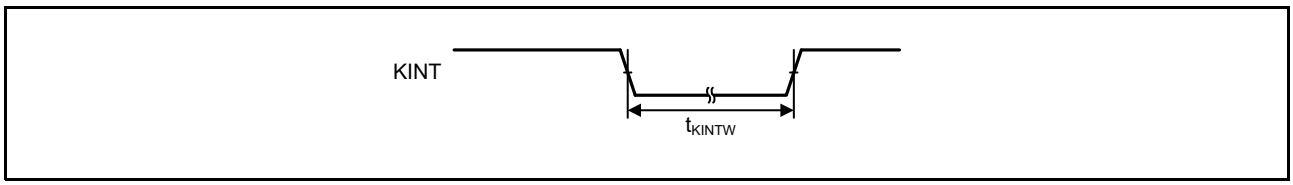


Figure 6.20 Key Interrupt Input Timing

6.3.6 I/O Ports, POE, GPT, and S14AD Trigger Timing

Table 6.21 I/O Ports, POE, GPT, and S14AD Trigger Timing

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width		t_{PRW}	2.5	—	—	t_{Pcyc}	Figure 6.21
	ELC event pulse input width			4	—	—		
POE	POE input trigger pulse width		t_{POEW}	1.5	—	—	t_{Pcyc}	Figure 6.22
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	—	—	t_{Pcyc}	Figure 6.23
		Both edges		2.5	—	—		
S14AD	14-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	—	—	t_{Pcyc}	Figure 6.24

Note 1. t_{Pcyc} refers to the period of a cycle of PCLKA for the GPT, and that of PCLKB for the I/O ports, POE, and S14AD.

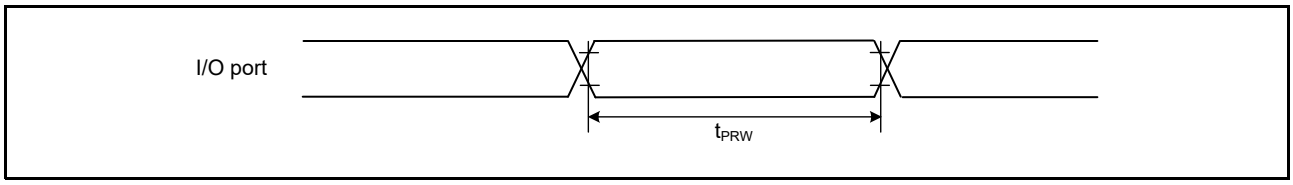


Figure 6.21 I/O Port Input Data Pulse Width

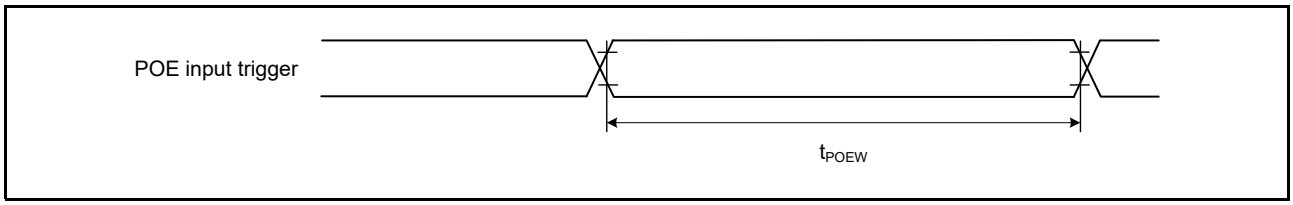


Figure 6.22 POE Input Trigger Pulse Width

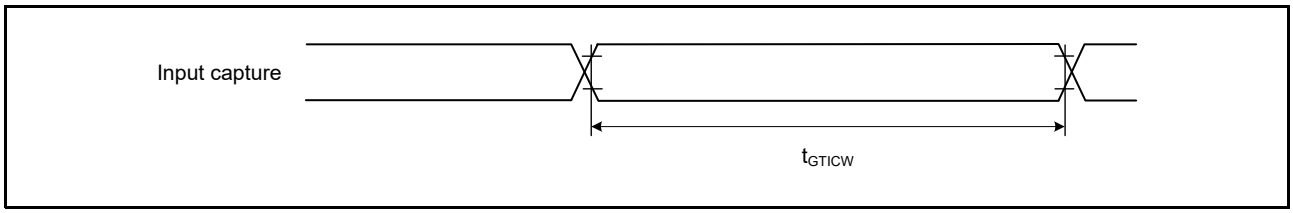


Figure 6.23 GPT Input Capture Pulse Width

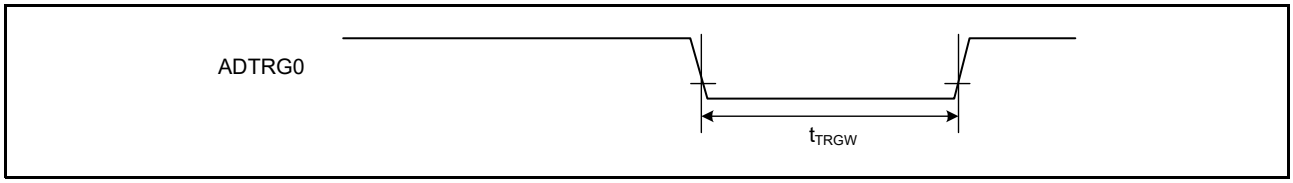


Figure 6.24 S14AD Trigger Input Timing

6.3.7 SCI Timing

Table 6.22 SCI Timing (1)
Conditions: High driving ability output is selected by the port drive capability bit in the PmnPFS register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
SCI	Frequency		pclkfmax	—	32	MHz	—
	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 6.25
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	1 × t_{Pcyc}	ns	
	Input clock fall time		t_{SCKf}	—	1 × t_{Pcyc}	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	6	—	t_{Pcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	1 × t_{Pcyc}	ns	
	Output clock fall time		t_{SCKf}	—	1 × t_{Pcyc}	ns	
	Transmit data delay time	Master	t_{TXD}	—	40	ns	Figure 6.26
		Slave		—	55		
	Receive data setup time	Master	t_{RXS}	45	—	ns	
		Slave		27	—		
	Receive data hold time	Master	t_{RXH}	5	—	ns	
		Slave		40	—		

Note 1. t_{Pcyc} refers to the period of a cycle of PCLKB.

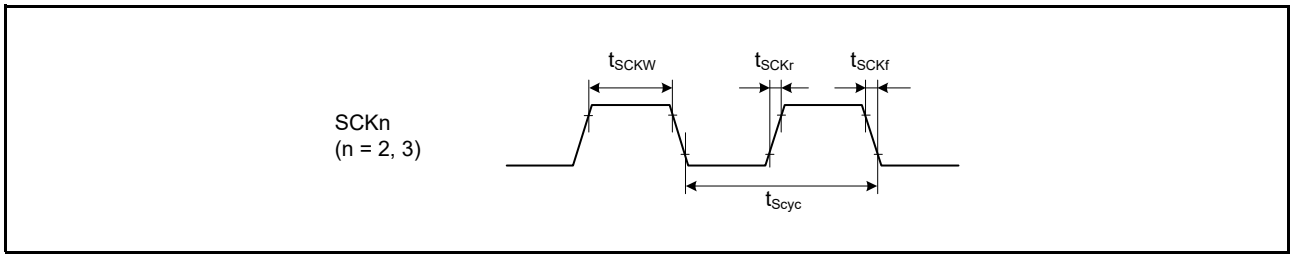


Figure 6.25 SCK Clock Input Timing

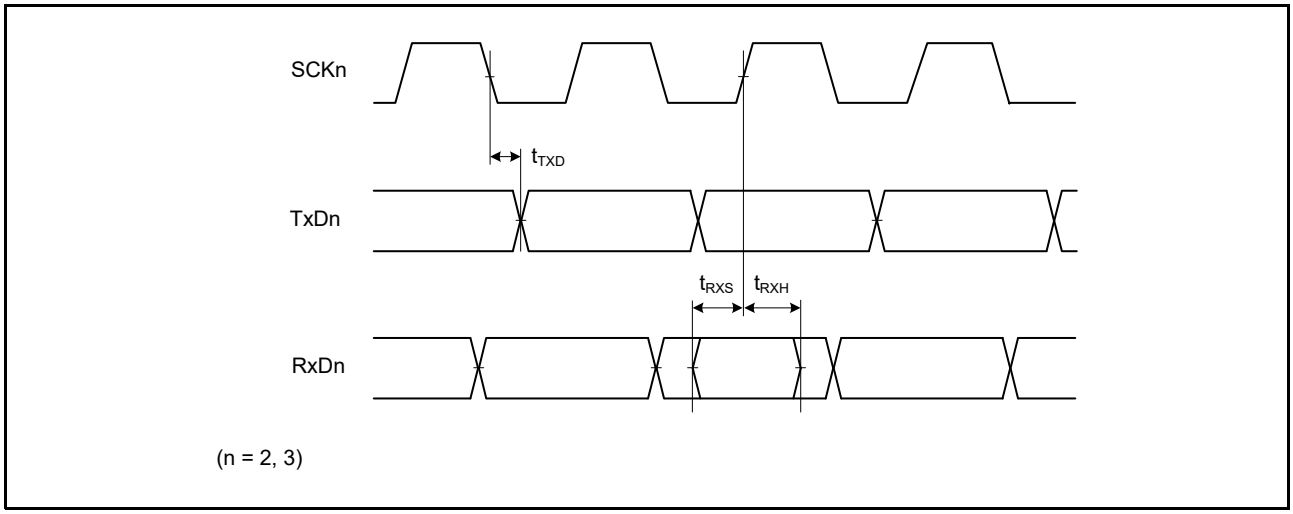


Figure 6.26 SCI Input and Output Timing in Clock Synchronous Mode

Table 6.23 SCI Timing (2)
Conditions: High driving ability output is selected by the port drive capability bit in the PmnPFS register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	Frequency		pclkfmax	—	32	MHz	—
	SCK clock cycle	Master	t_{SPcyc}	4	65536	t_{Pcyc}	Figure 6.27
		Slave		6	—		
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	1 × t_{Pcyc}	ns	
	Data input setup time	Master	t_{SU}	45	—	ns	Figure 6.28 to Figure 6.31
		Slave		27	—		
	Data input hold time	Master	t_H	33.3	—	ns	
		Slave		40	—		
	SS input setup time		t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time		t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time	Master	t_{OD}	—	40	ns	
		Slave		—	65		
	Data output hold time	Master	t_{OH}	–10	—	ns	
		Slave		–10	—		
	Data rise/fall time		t_{Dr}, t_{Df}	—	1 × t_{Pcyc}	ns	
	Slave access time	BOOST	t_{SA}	—	8	t_{Pcyc}	Figure 6.30, Figure 6.31
		NORMAL		—	6		
	Slave output release time	BOOST	t_{REL}	—	8	t_{Pcyc}	
		NORMAL		—	6		

Note 1. t_{Pcyc} refers to the period of a cycle of PCLKB.

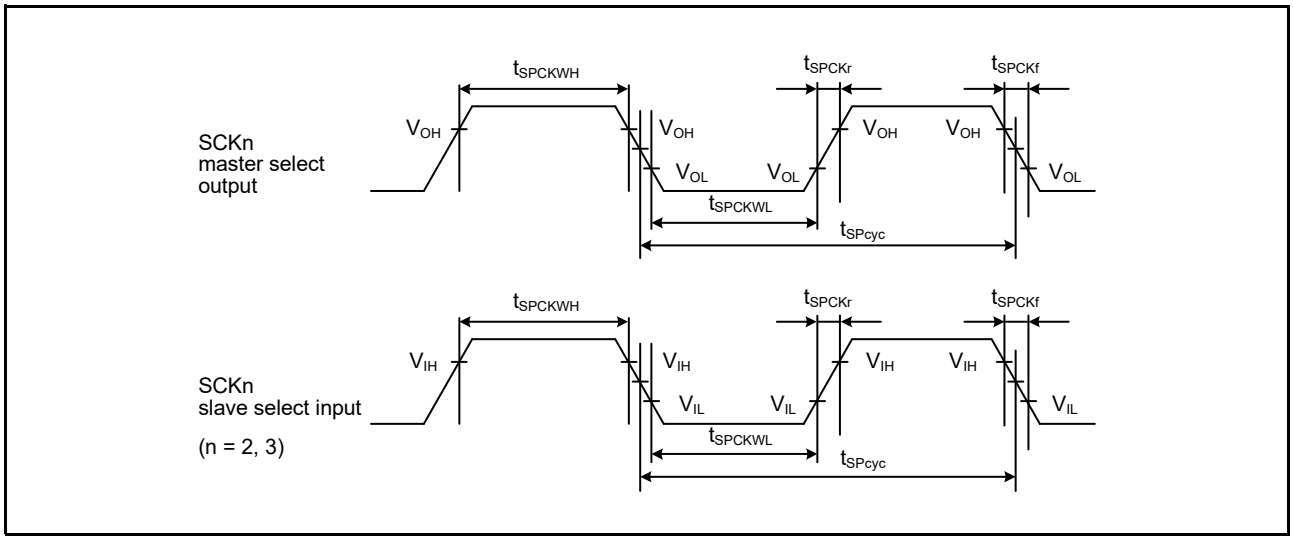


Figure 6.27 SCK Clock Input and Output Timing (Simple SPI Mode)

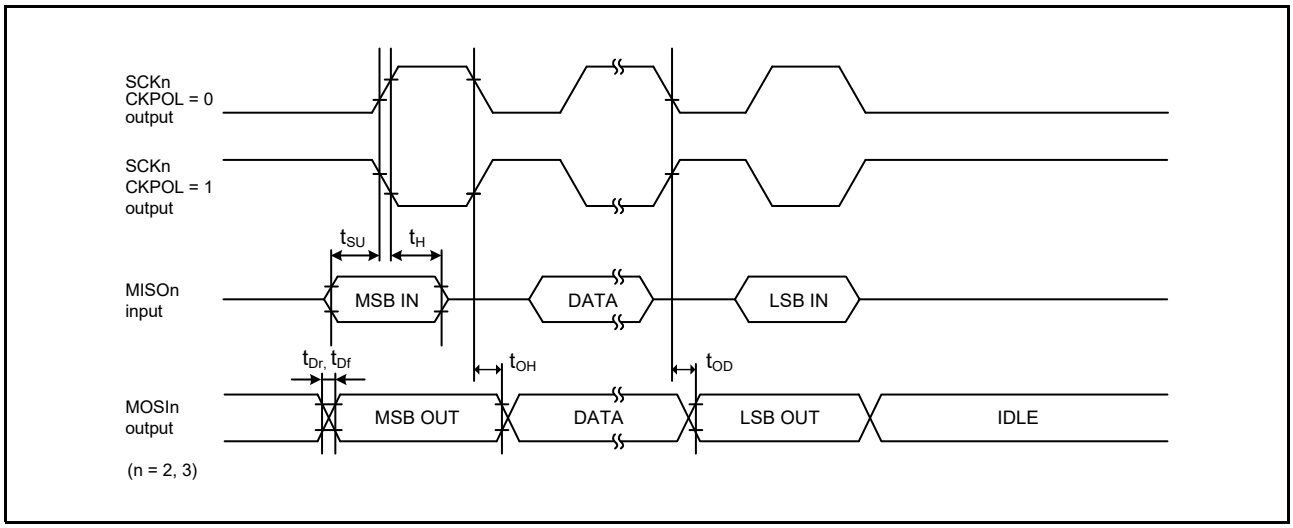


Figure 6.28 SCK Input and Output Timing (Simple SPI Mode) (Master, SPMR.CKPH = 1)

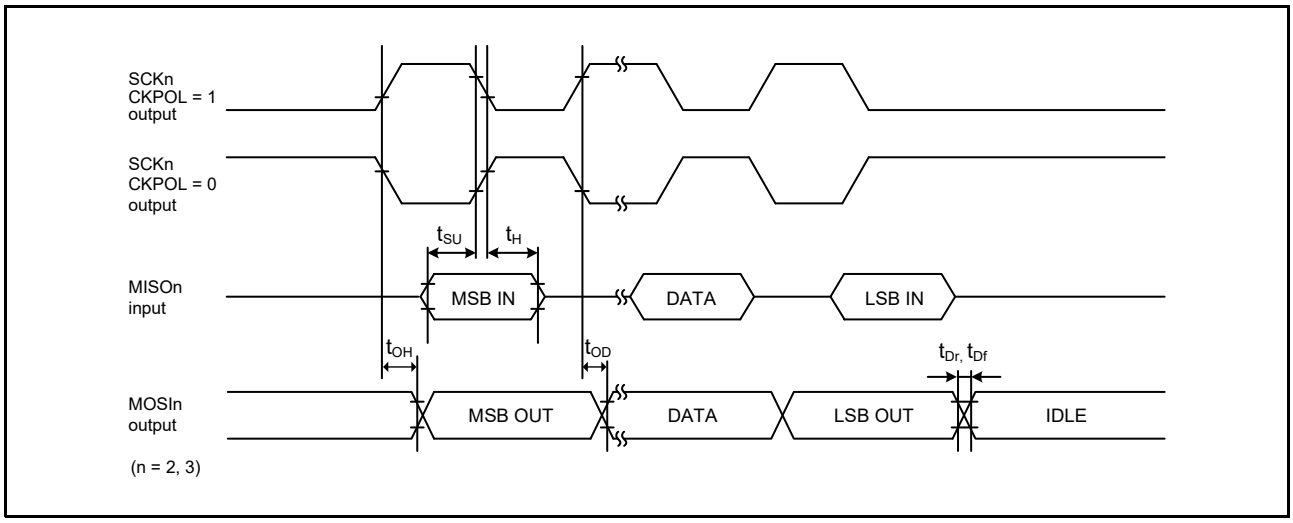


Figure 6.29 SCK Input and Output Timing (Simple SPI Mode) (Master, SPMR.CKPH = 0)

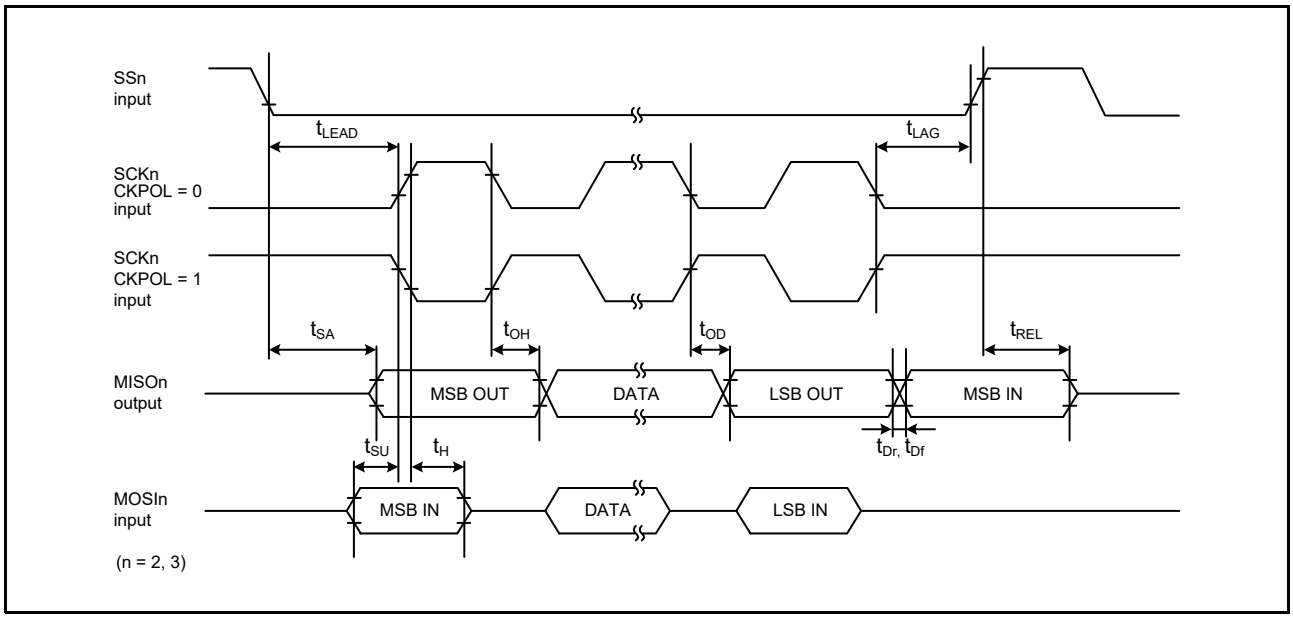


Figure 6.30 SCK Input and Output Timing (Simple SPI Mode) (Slave, SPMR.CKPH = 1)

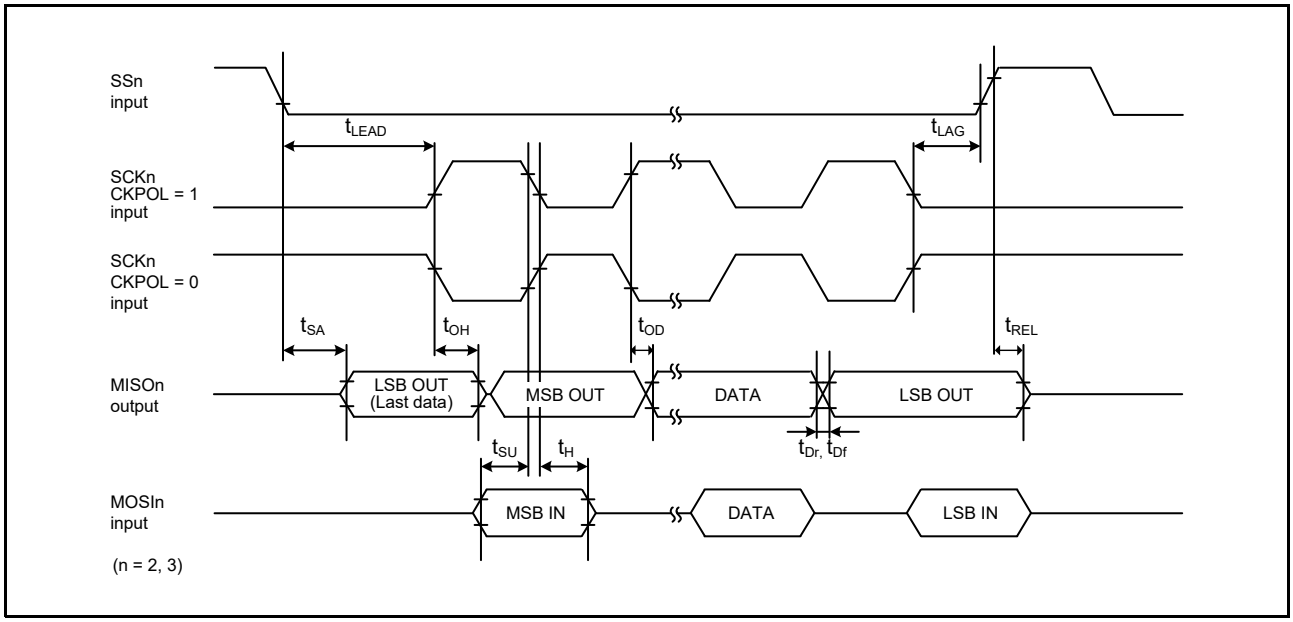
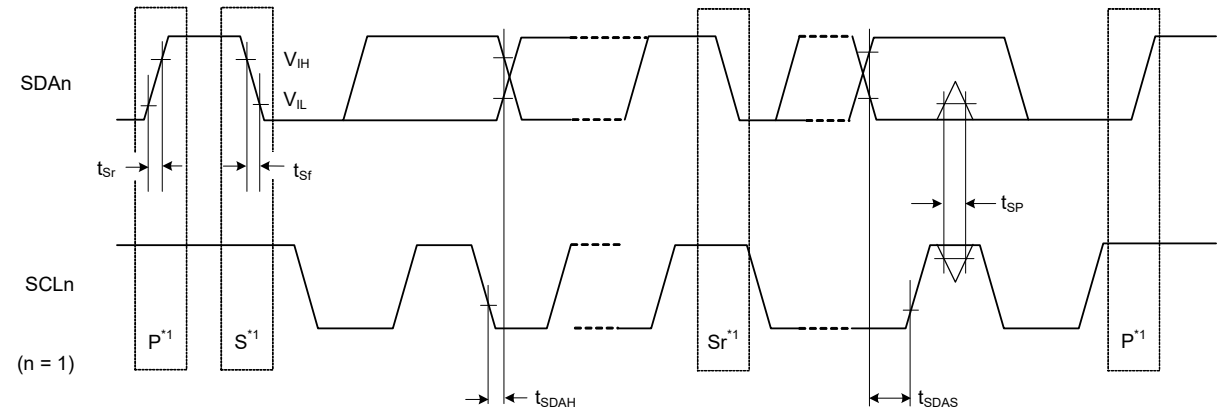


Figure 6.31 SCK Input and Output Timing (Simple SPI Mode) (Slave, SPMR.CKPH = 0)

Table 6.24 SCI Timing (3)
Conditions: High driving ability output is selected by the port drive capability bit in the PmnPFS register.

Item		Symbol	Min.	Max.*2	Unit	Test Conditions
Simple IIC (standard mode)	Frequency	pclkfmax	—	32	MHz	—
	SDA input rise time	t_{Sr}	—	1000	ns	Figure 6.32
	SDA input fall time	t_{Sf}	—	300	ns	
	SCL and SDA input spike pulse removal time	t_{SP}	0	4	t_{Pcyc}	Figure 6.32 SMR.CKS[1:0] = 00b, SNFR.NFCS[2:0] = 001b
				1024		Figure 6.32 SMR.CKS[1:0] = 11b, SNFR.NFCS[2:0] = 100b
	Data input setup time	t_{SDAS}	250	—	ns	Figure 6.32
	Data input hold time	t_{SDAH}	0	—	ns	
	SCl and SDA load capacitance	C_b*1	—	400	pF	
Simple IIC (fast mode)	Frequency	pclkfmax	—	32	MHz	—
	SCL and SDA input rise time	t_{Sr}	—	300	ns	Figure 6.32
	SCL and SDA input fall time	t_{Sf}	—	300	ns	
	SCL and SDA input spike pulse removal time	t_{SP}	0	4	t_{Pcyc}	Figure 6.32 SMR.CKS[1:0] = 00b, SNFR.NFCS[2:0] = 001b
				1024		Figure 6.32 SMR.CKS[1:0] = 11b, SNFR.NFCS[2:0] = 100b
	Data input setup time	t_{SDAS}	100	—	ns	Figure 6.32
	Data input hold time	t_{SDAH}	0	—	ns	
	SCl and SDA load capacitance	C_b*1	—	400	pF	

Note 1. Cb refers to the total capacitance of the bus line.
Note 2. t_{Pcyc} refers to the period of a cycle of PCLKB.



Note 1. S, P, and Sr indicate the following:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 6.32 SCK Input and Output Timing (Simple I2C Mode)

6.3.8 SPI Timing

Table 6.25 SPI Timing
Conditions: High driving ability output is selected by the port drive capability in the PmnPFS register.

Item				Symbol	Min.	Max.	Unit	Test Conditions
SPI	Frequency		BOOST	pclkfmax	—	64	MHz	—
			NORMAL		—	32		
	RSPCK clock cycle	Master	BOOST	t_{SPcyc}	4	4096	t_{Pcyc}	Figure 6.33
			NORMAL		2	4096		
		Slave			6	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$3 \times t_{Pcyc}$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$3 \times t_{Pcyc}$	—		
	RSPCK clock rise and fall time	Output		t_{SPCKr}, t_{SPCKf}	—	10	ns	Figure 6.33 IOVCCn ≥ 2.7 V
		Input			—	1	µs	
	Data input setup time	Master	BOOST	t_{SU}	25	—	ns	Figure 6.34 to Figure 6.39
			NORMAL		15	—		
		Slave			10	—		
	Data input hold time	Master		t_{HF}	0	—	ns	Figure 6.34 to Figure 6.37 The PCLKA division ratio is set to 1/2.
				t_{H}	1	—	t_{Pcyc}	Figure 6.34 to Figure 6.39 The PCLKA division ratio is set to any value other than 1/2.
		Slave			20	—	ns	Figure 6.34 to Figure 6.37
	SSL setup time	Master		t_{LEAD}	$-30 + N \times t_{SPcyc}$ *1	—	ns	
	SSL hold time	Master		t_{LAG}	$-30 + N \times t_{SPcyc}$ *2	—	ns	
	Data output delay time	Master		t_{OD}	—	14	ns	Figure 6.34 to Figure 6.39 IOVCCn ≥ 2.7 V
		Slave			—	50		
	Data output hold time	Master		t_{OH}	0	—	ns	Figure 6.34 to Figure 6.39
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	Figure 6.34 to Figure 6.37
	MOSI and MISO rise/fall time	Output		t_{Dr}, t_{Df}	—	10	ns	Figure 6.34 to Figure 6.39 IOVCCn ≥ 2.7 V
		Input			—	1	µs	Figure 6.34 to Figure 6.39
	SSL rise and fall time	Output		t_{SSLr}, t_{SSLf}	—	10	ns	Figure 6.34 to Figure 6.37 IOVCCn ≥ 2.7 V
		Input			—	1	µs	Figure 6.34 to Figure 6.37

Note: t_{Pcyc} refers to the period of a cycle of PCLKA.
Note 1. N indicates the RSPCK delay set in the SPCKD register.
Note 2. N indicates the RSPCK delay set in the SSLND register.

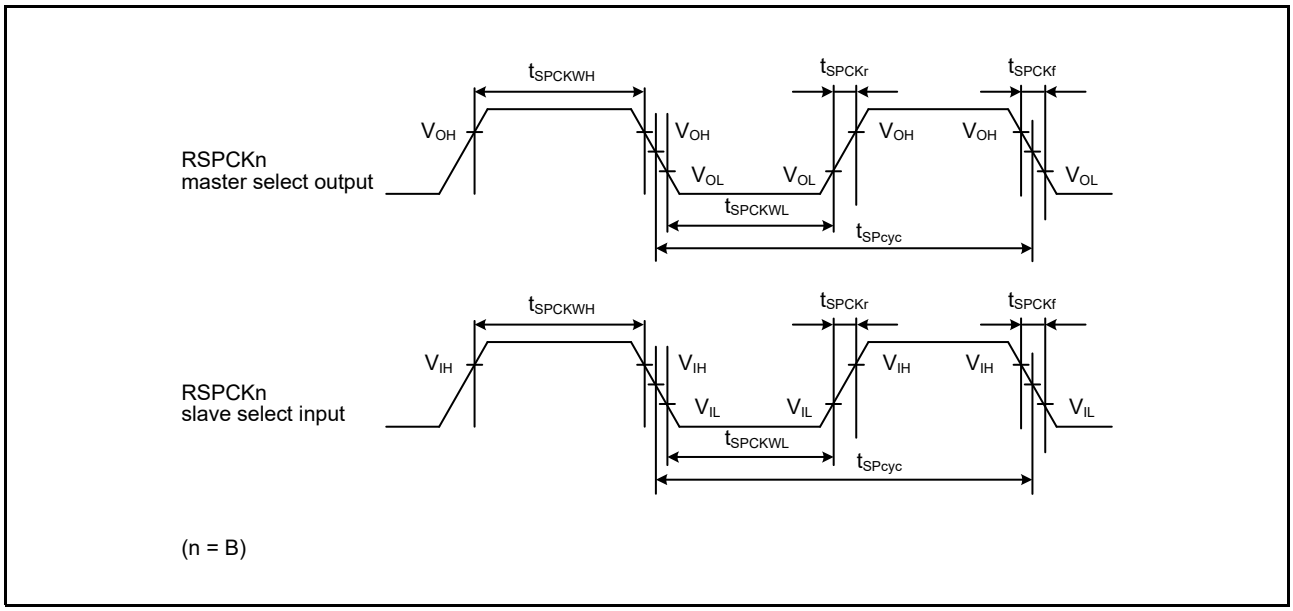


Figure 6.33 SPI Clock Timing

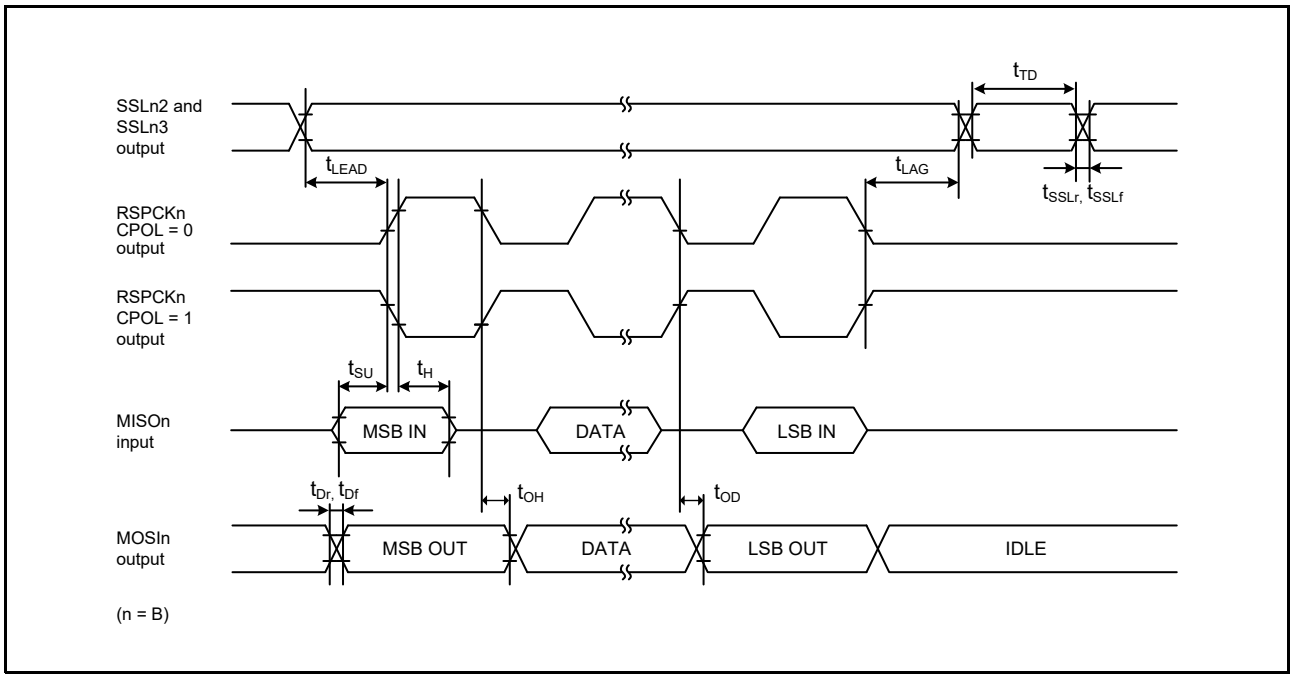


Figure 6.34 SPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio is Set to Any Value Other than 1/2)

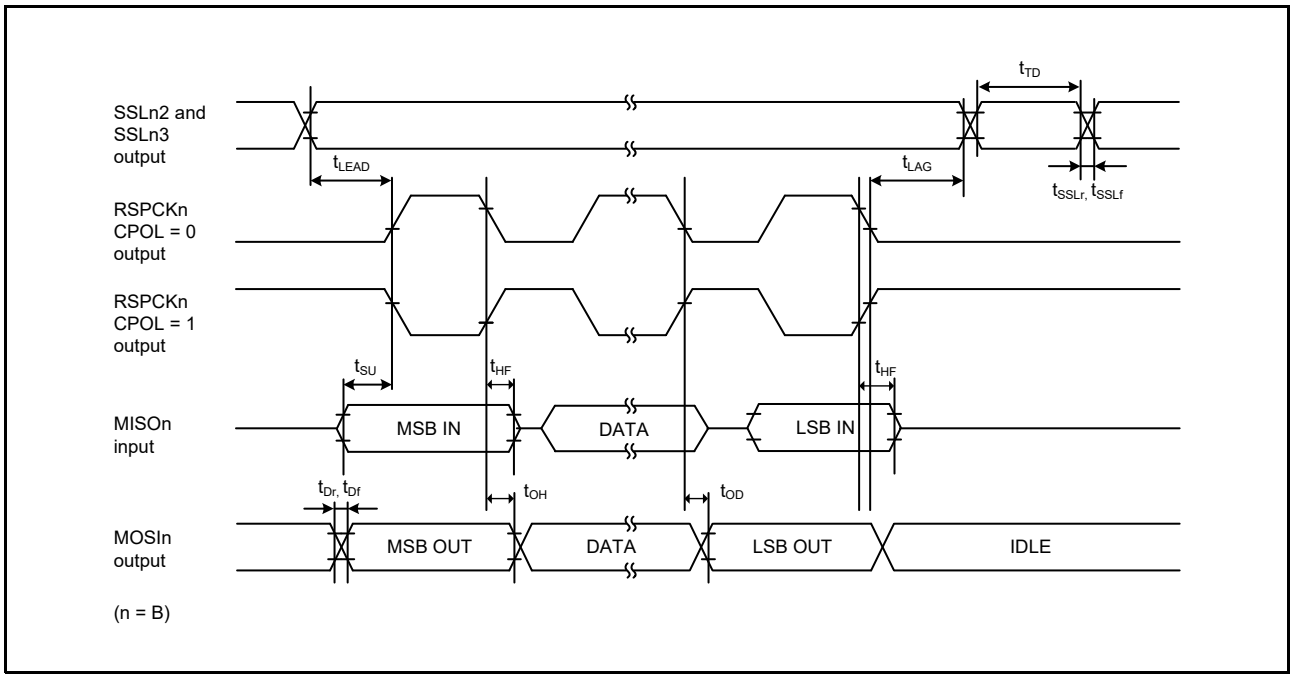


Figure 6.35 SPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio is Set to 1/2)

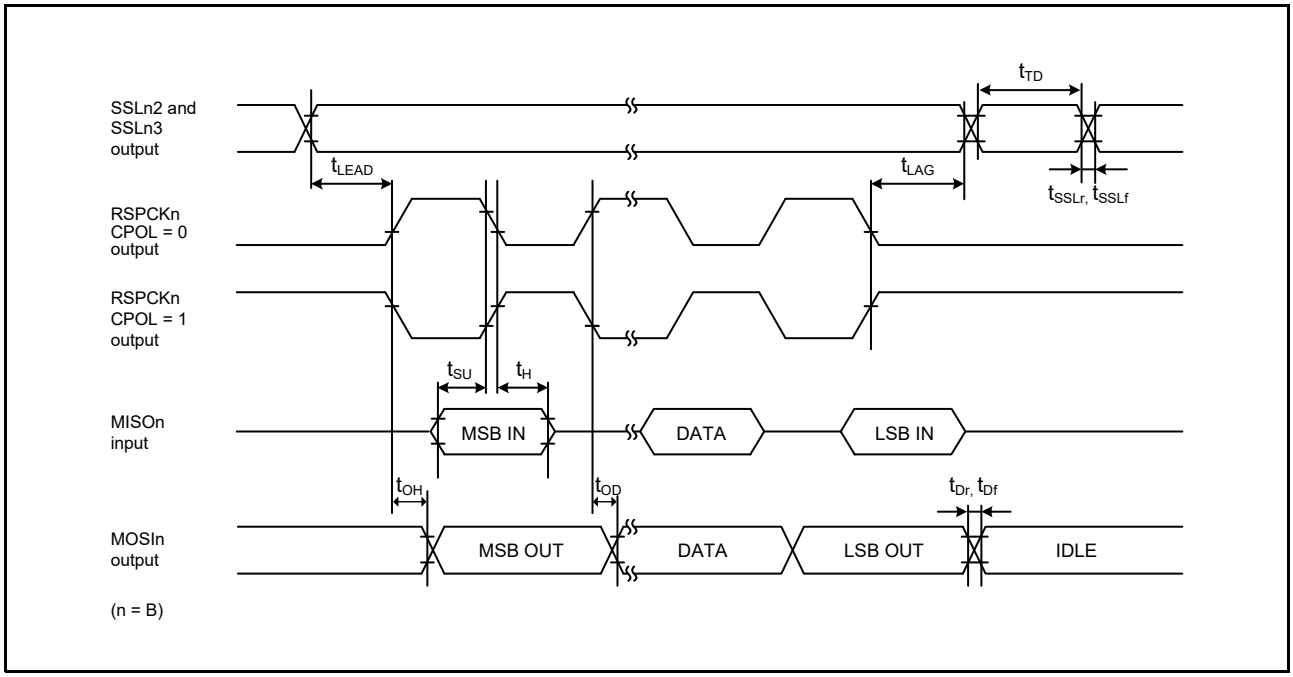


Figure 6.36 SPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio is Set to Any Value Other than 1/2)

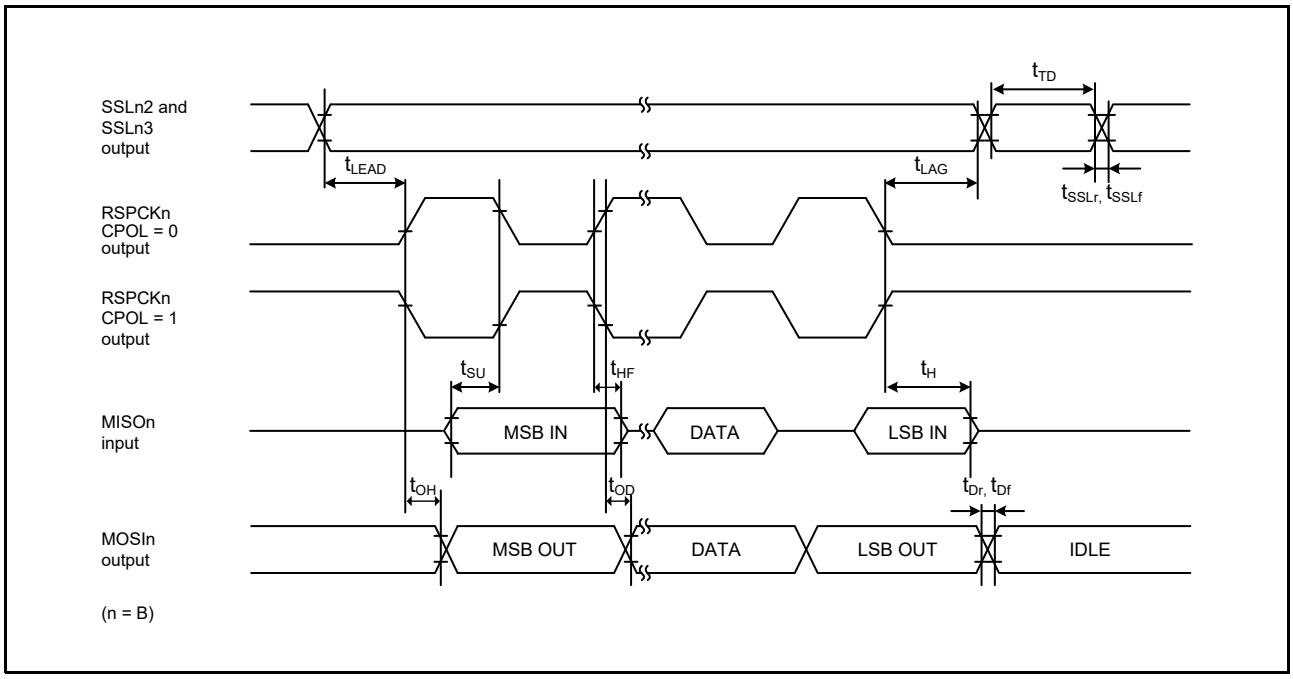


Figure 6.37 SPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio is Set to 1/2)

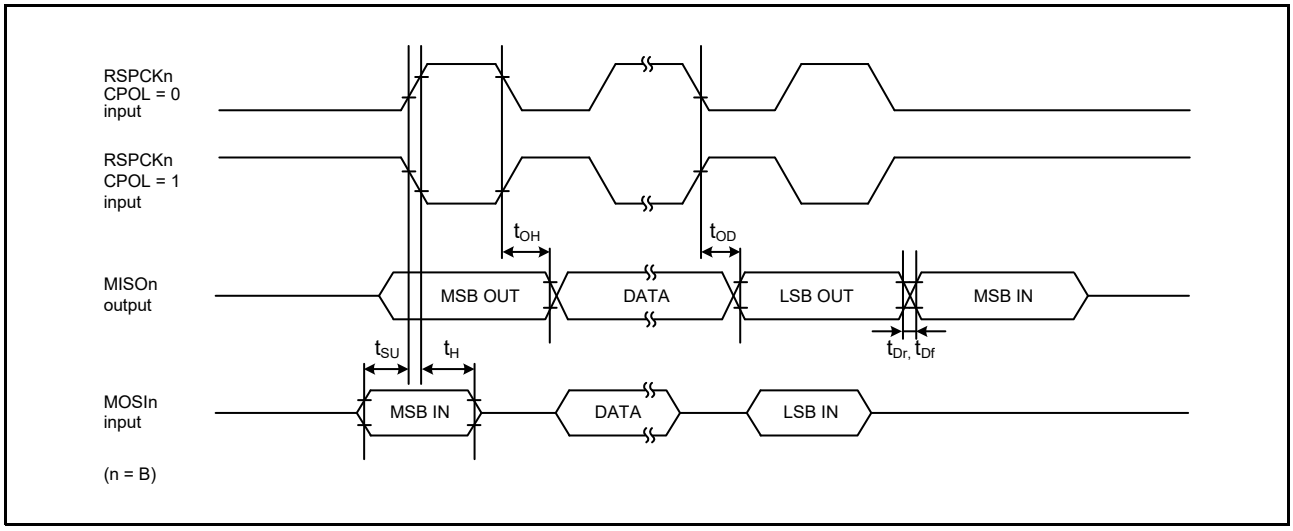


Figure 6.38 SPI Timing (Slave, CPHA = 0)

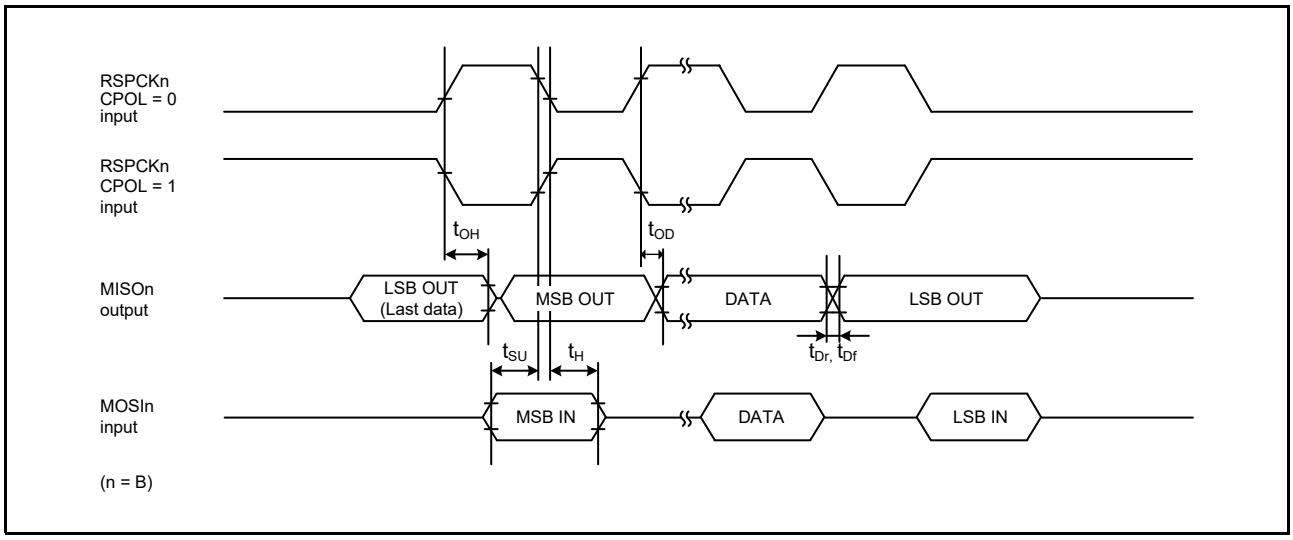


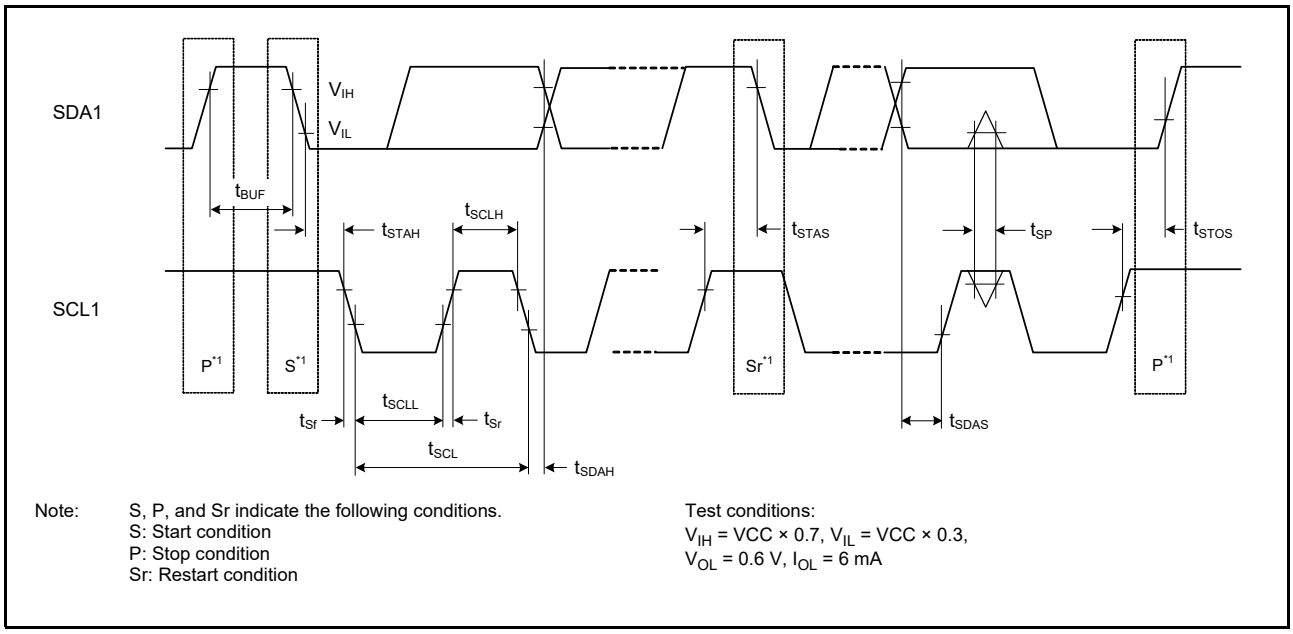
Figure 6.39 SPI Timing (Slave, CPHA = 1)

6.3.9 RIIC Timing

Table 6.26 RIIC Timing
Conditions: VCC = 3.0 to 3.6 V, V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3, V_{OL} = 0.6 V, I_{OL} = 6 mA
Standard driving ability output is selected in the port drive capability bit in the PmnPFS register.

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
RIIC (standard mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 6.40
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL and SDA input rise time	t_{Sr}	—	1000	ns	
	SCL and SDA input fall time	t_{Sf}	—	300	ns	
	SCL and SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL and SDA load capacitance*2	C_b	—	400	pF	
RIIC (fast mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 6.40
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL and SDA input rise time	t_{Sr}	—	300	ns	
	SCL and SDA input fall time	t_{Sf}	—	300	ns	
	SCL and SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL and SDA load capacitance*2	C_b	—	400	pF	

Note: t_{IICcyc} refers to the period of a cycle of RIIC internal reference clock (IICφ).
Note 1. The values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled by setting the ICFER.NFE bit to 1.
Note 2. C_b refers to the total capacitance of the bus line.



Note: S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions:
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3,
V_{OL} = 0.6 V, I_{OL} = 6 mA

Figure 6.40 I²C Bus Interface Input and output Timing

6.3.10 CLKOUT Timing

Table 6.27 CLKOUT Timing

Item		Symbol	Min.	Max.	Unit	Test Conditions
CLKOUT32	CLKOUT32K pin output cycle	t_{Ccyc}	30.5	—	µs	Figure 6.41

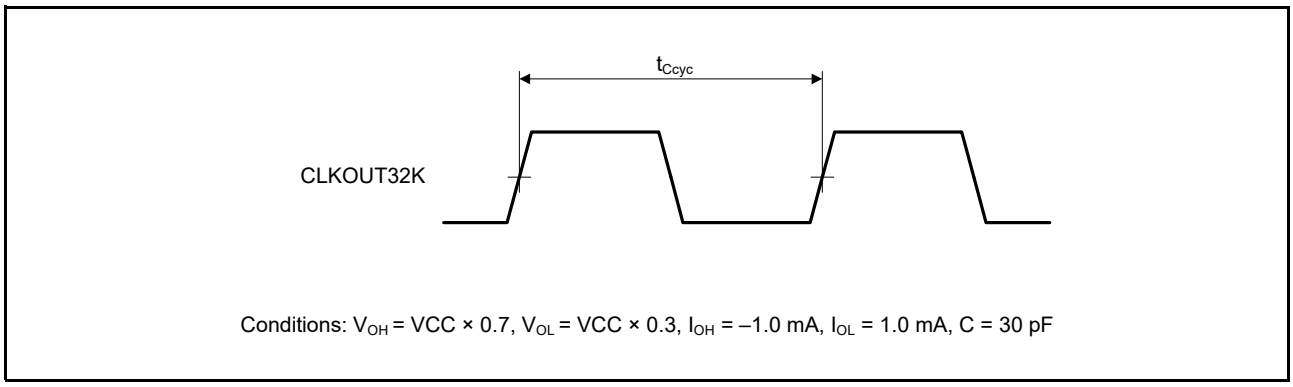


Figure 6.41 CLKOUT Output Timing

6.3.11 TMR Timing

Table 6.28 TMR Timing

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
TMR	Pulse width of the timer clock	Single edge specified	t_{TMCWH}, t_{TMCWL}	1.5	—	—	t_{Pcyc}	Figure 6.42
		Both edges specified		2.5	—	—		

Note 1. t_{Pcyc} refers to the period of a cycle of PCLKB.

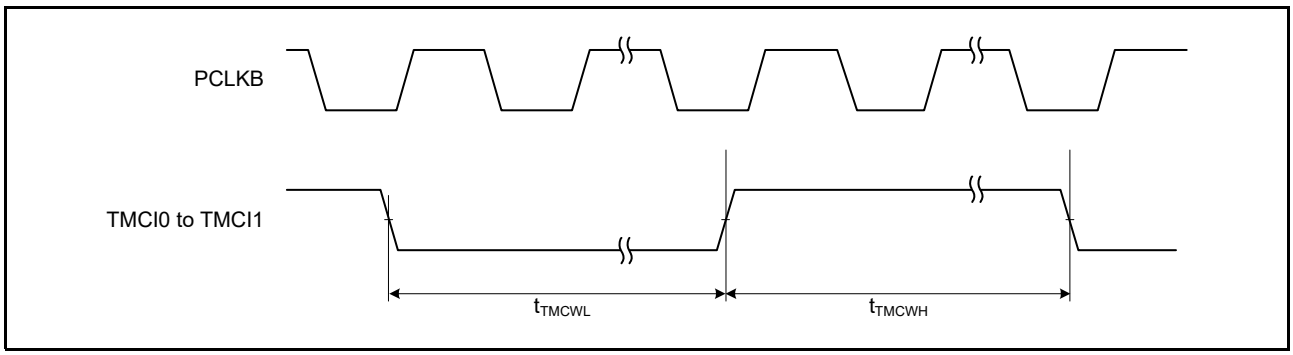


Figure 6.42 TMR Clock Input Timing

6.4 A/D Conversion Characteristics

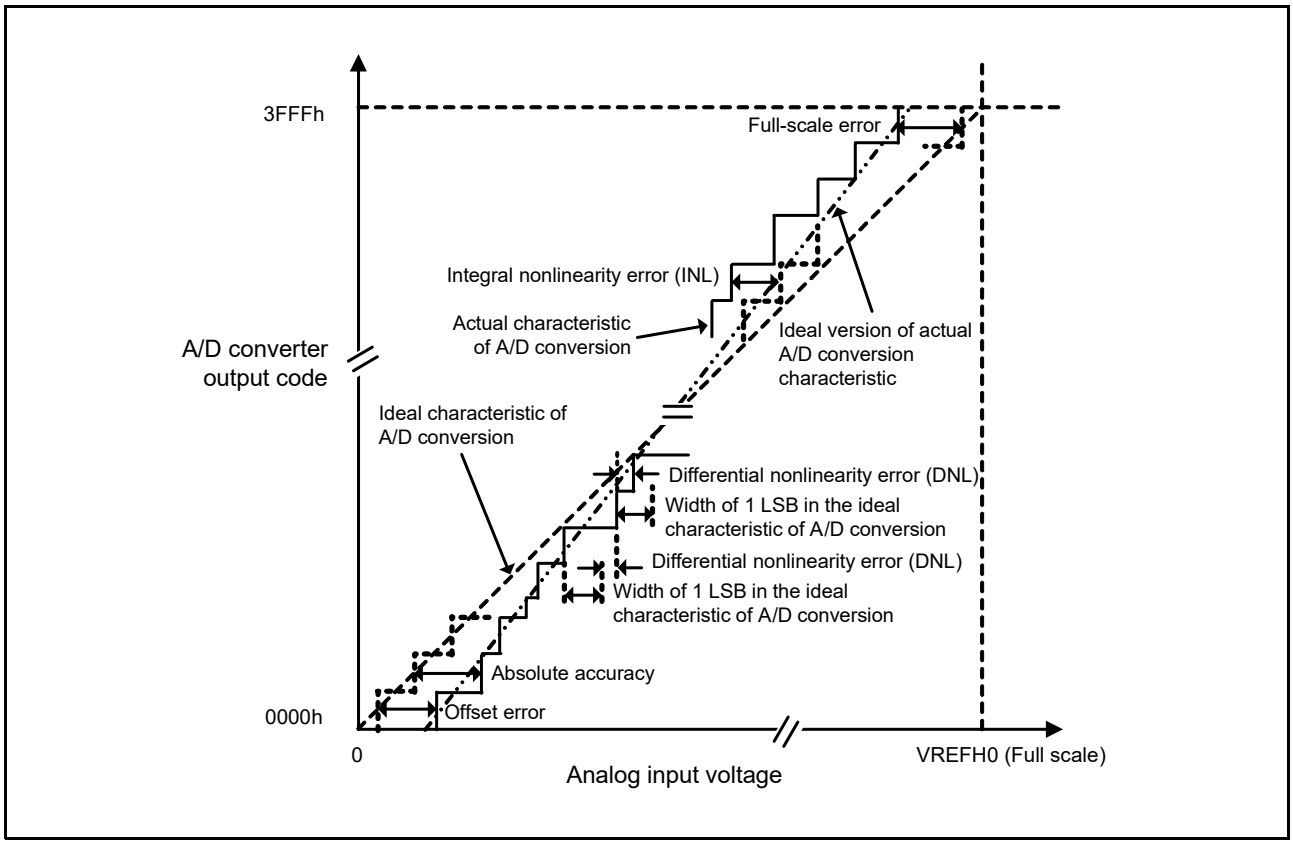


Figure 6.43 Terminology for Characteristics of an A/D Converter

Absolute accuracy

Absolute accuracy is a measure of the difference between the output codes which would be produced by an ideal A/D converter and the codes output by the actual A/D converter. Absolute accuracy is measured by the differences between the codes at the central points (within 1 LSB) of the ranges of analog input voltage for which given digital codes would be expected in ideal A/D conversion. For example, when the resolution is 14 bits and the reference voltage (VREFH0) is 3.276 V, the width of 1 LSB is 0.2 mV, and analog inputs including 0, 0.2, 0.4 mV, and so on, can be used.
An absolute accuracy of ± 5 LSB means that where an ideal A/D converter would output 0008h when the analog input voltage is 1.6 mV, the result from the actual A/D converter can be any value in the range from 0003h to 000Dh.

Integral nonlinearity error (INL)

Integral nonlinearity error is a measure of the maximum deviation between the ideal linear variation in output values with voltage and the actual measured output codes when the measured offset error and full-scale error are 0.

Differential nonlinearity error (DNL)

Differential nonlinearity error is a measure of the difference between the width of 1 LSB in an ideal A/D converter and the actual measured output codes.

Offset error

Offset error is a measure of the difference between the point at which the first ideal output code changes and the first actual measured output code.

Full-scale error

Full-scale error is a measure of the difference between the point at which the ideal output code changes to the last code and the last actual measured code.

We do not inspect the characteristics of the A/D converter before shipment unless otherwise stated. The values presented in this manual are only for reference. The electrical characteristics values that are given are categorized into the following seven groups.

(1) AVCC0 = VREFH0 = 2.7 to 3.6 V
Note that the values in the column “Max.” in Table 6.29 only apply in the case of a normal distribution with ±3σ variation from the mean.
(2) AVCC0 = VREFH0 = 2.7 to 3.6 V
(3) AVCC0 = VREFH0 = 2.4 to 3.6 V
(4) AVCC0 = VREFH0 = 1.8 to 3.6 V
(5) AVCC0 = VREFH0 = 1.62 to 3.6 V
(6) AVCC0 = 3.3 V, AVTRO = 2.5 V (the output of the reference voltage generator is used for reference)
(7) AVCC0 = 1.8 V, AVTRO = 1.25 V (the output of the reference voltage generator is used for reference)

Some points to note regarding the electrical characteristics of the A/D converter are listed below.
(1) The characteristics do not include the quantization error (±0.5 LSB).
(2) The characteristics are the values after offset calibration.
(3) The characteristics only apply when the 14-bit A/D converter pins are in use for A/D conversion, and not for any other functions.
(4) The conversion time (t_{CONV}) is the sum of the sampling time (t_{SPL}) and time for conversion by successive approximation (t_{SAM}).
The values in parentheses in the conversion time indicate the sampling time.

Table 6.29 A/D Conversion Characteristics (1)
Conditions: AVCC0 = VREFH0 = 2.7 to 3.6 V

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	32*3	MHz	ADSCLKCR.SCLKEN = 0
		—	32.768	—	kHz	ADSCLKCR.SCLKEN = 1
Dynamic range	A_{in}	0	—	VREFH0	V	—
Resolution		12	—	14	Bit	—
Conversion time	Permissible signal source impedance Max. = 0.5 kΩ	1.0 (0.46875)	—	—	µs	High-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 0Fh
		1.5 (0.96875)	—	—	µs	Standard-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 1Fh
		593.75 (60.98)	—	—	µs	ADSCLKCR.SCLKEN = 1 ADSSTRn.SST[7:0] = 02h
Offset error*1		–1.2	—	1.2	mV	High-precision channel
Full-scale error*1		–1.2	—	1.2	mV	High-precision channel
Absolute accuracy*1		—	±4.0*2	±11	LSB	High-precision channel
DNL differential nonlinearity error*1		—	±1.0*2	±1.5	LSB	High-precision channel
INL integral nonlinearity error*1		—	±2.5	±4.0	LSB	High-precision channel
ENOB (effective number of bits) error*1, *2		—	13	—	Bit	High-precision channel

Note 1. The values apply when the averaging mode is enabled, averaging of 16 results of conversion is selected (ADADC = 85h), and the conversion resolution is set to 14 bits (ADCER.ADPRC[1:0] = 11b).
Note 2. The value applies when AVCC0 = VREFH0 = 3.3 V.

Note 3. If AVCC0 ≠ VREFH0, the condition AVCC0 ≥ VREFH0 ≥ 2.7 V applies.

Table 6.30 A/D Conversion Characteristics (2)
Conditions: AVCC0 = VREFH0 = 2.7 to 3.6 V

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	32*3	MHz	ADSCLKCR.SCLKEN = 0
		—	32.768	—	kHz	ADSCLKCR.SCLKEN = 1
Dynamic range	A_{in}	0	—	VREFH0	V	—
Resolution		12	—	14	Bit	—
Conversion time	Permissible signal source impedance Max. = 0.5 kΩ	1.0 (0.46875)	—	—	µs	High-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 0Fh
		1.5 (0.96875)	—	—	µs	Standard-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 1Fh
		593.75 (60.98)	—	—	µs	ADSCLKCR.SCLKEN = 1 ADSSTRn.SST[7:0] = 02h
Offset error*1		–1.7	—	1.7	LSB	High-precision channel
Full-scale error*1		–1.7	—	1.7	LSB	High-precision channel
Absolute accuracy*1		—	±4.0*2	±14	LSB	High-precision channel
DNL differential nonlinearity error*1		—	±1.0*2	±1.7	LSB	High-precision channel
INL integral nonlinearity error*1		—	±2.5	±5.0	LSB	High-precision channel
ENOB (effective number of bits) error*1, *2		—	13	—	Bit	High-precision channel

Note 1. The values apply when the averaging mode is enabled, averaging of 16 results of conversion is selected (ADADC = 85h), and the conversion resolution is set to 14 bits (ADCER.ADPRC[1:0] = 11b).
Note 2. The value applies when AVCC0 = VREFH0 = 3.3 V.
Note 3. If AVCC0 ≠ VREFH0, the condition AVCC0 ≥ VREFH0 ≥ 2.7 V applies.

Table 6.31 A/D Conversion Characteristics (3)
Conditions: AVCC0 = VREFH0 = 2.4 to 3.6 V

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	16*3	MHz	ADSCLKCR.SCLKEN = 0
		—	32.768	—	kHz	ADSCLKCR.SCLKEN = 1
Dynamic range	A_{in}	0	—	VREFH0	V	—
Resolution		12	—	14	Bit	—
Conversion time	Permissible signal source impedance Max. = 0.5 kΩ	2.0 (0.9375)	—	—	µs	High-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 0Fh
		3.0 (1.9375)	—	—	µs	Standard-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 1Fh
		593.75 (60.98)	—	—	µs	ADSCLKCR.SCLKEN = 1 ADSSTRn.SST[7:0] = 02h
Offset error*1		–1.7	—	1.7	mV	High-precision channel
Full-scale error*1		–1.7	—	1.7	mV	High-precision channel
Absolute accuracy*1		—	±4.0*2	±14	LSB	High-precision channel
DNL differential nonlinearity error*1		—	±1.0*2	±1.7	LSB	High-precision channel
INL integral nonlinearity error*1		—	±2.5	±5.0	LSB	High-precision channel
ENOB (effective number of bits) error*1, *2		—	13	—	Bit	High-precision channel

Note 1. The values apply when the averaging mode is enabled, averaging of 16 results of conversion is selected (ADADC = 85h), and the conversion resolution is set to 14 bits (ADCER.ADPRC[1:0] = 11b).
Note 2. The value applies when AVCC0 = VREFH0 = 3.3 V.
Note 3. If AVCC0 ≠ VREFH0, the condition AVCC0 ≥ VREFH0 ≥ 2.4 V applies.

Table 6.32 A/D Conversion Characteristics (4)
Conditions: AVCC0 = VREFH0 = 1.8 to 3.6 V

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8*2	MHz	ADSCLKCR.SCLKEN = 0
		—	32.768	—	kHz	ADSCLKCR.SCLKEN = 1
Dynamic range	A_{in}	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time	Permissible signal source impedance Max. = 0.5 kΩ	3.75 (1.875)	—	—	µs	High-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 0Fh
		5.75 (3.875)	—	—	µs	Standard-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 1Fh
		531.25 (60.98)	—	—	µs	ADSCLKCR.SCLKEN = 1 ADSSTRn.SST[7:0] = 02h
Offset error*1		–1.7	—	1.7	mV	High-precision channel
Full-scale error*1		–1.7	—	1.7	mV	High-precision channel
Absolute accuracy*1		—	±2.0	±7.0	LSB	High-precision channel
DNL differential nonlinearity error*1		—	±1.0	±2.0	LSB	High-precision channel
INL integral nonlinearity error*1		—	±1.0	±3.0	LSB	High-precision channel

Note 1. The values apply when the averaging mode is disabled and the conversion resolution is set to 12 bits (ADCER.ADPRC[1:0] = 00h).
Note 2. If AVCC0 ≠ VREFH0, the condition AVCC0 ≥ VREFH0 ≥ 1.8 V applies.

Table 6.33 A/D Conversion Characteristics (5)
Conditions: AVCC0 = VREFH0 = 1.62 to 3.6 V

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8*3	MHz	ADSCLKCR.SCLKEN = 0
		—	32.768	—	kHz	ADSCLKCR.SCLKEN = 1
Dynamic range	A_{in}	0	—	VREFH0	V	—
Resolution*1		—	—	10	Bit	—
Conversion time	Permissible signal source impedance Max. = 0.5 kΩ	3.75 (1.875)	—	—	µs	High-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 0Fh
		5.75 (3.875)	—	—	µs	Standard-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 1Fh
		531.25 (60.98)	—	—	µs	ADSCLKCR.SCLKEN = 1 ADSSTRn.SST[7:0] = 02h
Offset error*2		–1.7	—	1.7	mV	High-precision channel
Full-scale error*2		–1.7	—	1.7	mV	High-precision channel
Absolute accuracy*2		—	±0.5	±2.5	LSB	High-precision channel
DNL differential nonlinearity error*2		—	±0.5	±1.5	LSB	High-precision channel
INL integral nonlinearity error*2		—	±0.5	±1.5	LSB	High-precision channel

Note 1. Due to selection of the 12-bit resolution, ignore the two lower-order bits of the 14-bit result of A/D conversion (in the ADDRy registers).
Note 2. The values apply when the averaging mode is disabled and the conversion resolution is set to 12 bits (ADCER.ADPRC[1:0] = 00h).
Note 3. If AVCC0 ≠ VREFH0, the condition AVCC0 ≥ VREFH0 ≥ 1.62 V applies.

Table 6.34 Characteristics of A/D Conversion when the Output Value from the Reference Voltage Generation Circuit is in Use as the Reference Voltage (1)

Conditions: AVCC0 = 3.3 V, AVTRO = 2.50 V

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	16	MHz	ADSCLKCR.SCLKEN = 0
		—	32.768	—	kHz	ADSCLKCR.SCLKEN = 1
Dynamic range	A_{in}	0	—	VREFH0	V	—
Resolution		12	—	14	Bit	—
Conversion time	Permissible signal source impedance Max. = 0.5 kΩ	2.0 (0.9375)	—	—	µs	High-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 0Fh
		3.0 (1.9375)	—	—	µs	Standard-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 1Fh
		593.75 (60.98)	—	—	µs	ADSCLKCR.SCLKEN = 1 ADSSTRn.SST[7:0] = 02h
Offset error*1		–1.7	—	1.7	mV	High-precision channel
DNL differential nonlinearity error*1		—	±1.5	—	LSB	High-precision channel
INL integral nonlinearity error*1		—	±3.0	—	LSB	High-precision channel

Note 1. The values apply when the averaging mode is enabled, averaging of 16 results of conversion is selected (ADADC = 85h), and the conversion resolution is set to 14 bits (ADCER.ADPRC[1:0] = 11b).

Table 6.35 Characteristics of A/D Conversion when the Output Value from the Reference Voltage Generation Circuit is in Use as the Reference Voltage (2)

Conditions: AVCC0 = 1.8 V, AVTRO = 1.25 V

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8	MHz	ADSCLKCR.SCLKEN = 0
		—	32.768	—	kHz	ADSCLKCR.SCLKEN = 1
Dynamic range	A_{in}	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time	Permissible signal source impedance Max. = 0.5 kΩ	3.75 (1.875)	—	—	µs	High-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 0Fh
		5.75 (3.875)	—	—	µs	Standard-precision channel ADSCLKCR.SCLKEN = 0 ADSSTRn.SST[7:0] = 1Fh
		531.25 (60.98)	—	—	µs	ADSCLKCR.SCLKEN = 1 ADSSTRn.SST[7:0] = 02h
Offset error*1		–1.7	—	1.7	mV	High-precision channel
DNL differential nonlinearity error*1		—	±1.0	—	LSB	High-precision channel
INL integral nonlinearity error*1		—	±1.0	—	LSB	High-precision channel

Note 1. The values apply when the averaging mode is disabled and the conversion resolution is set to 12 bits (ADCER.ADPRC[1:0] = 00h).

6.5 Temperature Sensor Characteristics

Table 6.36 Temperature Sensor Characteristics

Item	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	±5	—	°C	AVCC0 ≥ 2.6 V
	—	±6	—	°C	AVCC0 < 2.6 V
Temperature gradient	—	1.6	—	mV/°C	—
Temperature sensor activation time	—	30	120	µs	—
Sampling time	—	2	7	µs	—

Note: We do not inspect the characteristics of the temperature sensor before shipment. The values presented in this manual are only for reference.

6.6 VREF Characteristics

Table 6.37 VREF Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output voltage	AVTRO	1.17	1.25	1.33	V	AVCC0 ≥ 2.8 V VREF.AVCR.AVSEL = 0
	AVTRO	2.34	2.50	2.66	V	AVCC0 ≥ 2.8 V VREF.AVCR.AVSEL = 1
	AVTRO	1.17	1.25	1.33	V	AVCC0 < 2.8 V VREF.AVCR.AVSEL = 0
Waiting time till the circuit activates and operation is stable	t_{VRSTUP}	—	—	50	ms	—

Note: We do not inspect the VREF characteristics before shipment. The values presented in this manual are only for reference.

6.7 Oscillation Stop Detection Circuit Characteristics

Table 6.38 Oscillation Stop Detection Circuit Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	30	µs	Figure 6.44

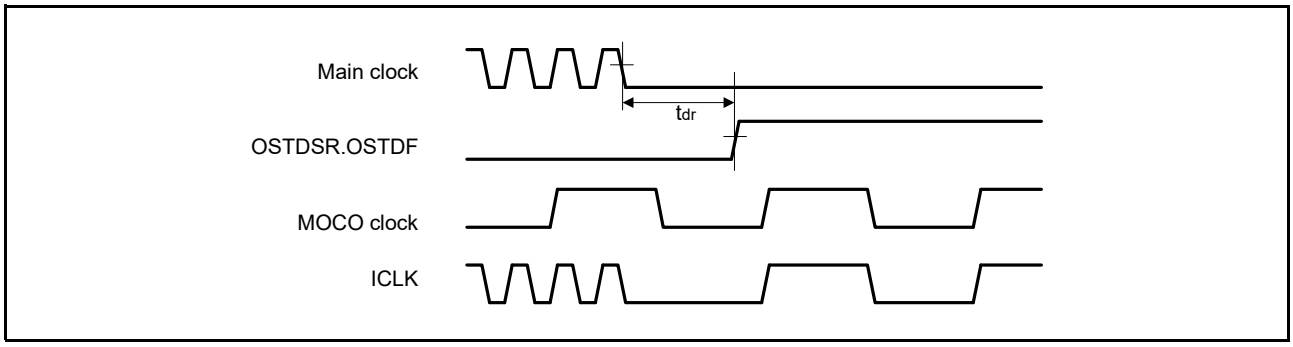


Figure 6.44 Oscillation Stop Detection Timing

6.8 Characteristics of Power-on Reset Circuit and Low Voltage Detection Circuit

Table 6.39 Characteristics of Power-on Reset Circuit and Low Voltage Detection Circuit

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset circuit (POR)	Rising	V_{POR}	1.40	1.50	1.60	V	Figure 6.45
		Falling	V_{PORL}	1.30	1.40	1.50		
	Voltage monitoring 0 circuit (LVD0)		V_{det0_0}	2.34	2.42	2.50	V	Figure 6.46
			V_{det0_1}	2.10	2.17	2.24		
			V_{det0_2}	1.86	1.92	1.98		
			V_{det0_3}	1.62	1.67	1.72		
	Voltage monitoring 1 circuit (LVD1)		V_{det1_0}	2.74	2.83	2.92	V	Figure 6.47
			V_{det1_1}	2.58	2.66	2.74		
			V_{det1_3}	2.42	2.50	2.58		
			V_{det1_5}	2.26	2.33	2.40		
			V_{det1_7}	2.10	2.17	2.24		
			V_{det1_9}	1.94	2.00	2.06		
			V_{det1_B}	1.78	1.84	1.90		
			V_{det1_D}	1.62	1.67	1.72		
	Voltage monitoring BAT circuit (LVDBAT)		V_{detBAT_5}	2.26	2.33	2.40	V	Figure 6.48
			V_{detBAT_7}	2.10	2.17	2.24		
			V_{detBAT_9}	1.94	2.00	2.06		
			V_{detBAT_B}	1.78	1.84	1.90		
			V_{detBAT_D}	1.62	1.67	1.72		
Internal reset time	LVD0 reset time		t_{LVD0}	—	3.10	—	ms	Figure 6.46
	LVD1 reset time		t_{LVD1}	—	1.38	—	ms	Figure 6.47
	LVDBAT reset time		t_{LVDBAT}	—	1.38	—	ms	Figure 6.48
Minimum VCC down time*1			t_{VOFF}	4	—	—	ms	Figure 6.45 to Figure 6.48
LVD0 response delay time			t_{det}	—	150	300	µs	Figure 6.46 to Figure 6.48
LVD1 response delay time			t_{det}	—	150	300	µs	
LVDBAT response delay time (when the VCC and VBAT_EHC pins are connected)			t_{det}	—	150	300	µs	
LVDBAT response delay time (when the VCC and VBAT_EHC pins are not connected)			t_{det}	—	400	800	µs	
LVD1 operation stabilization time (after the LVD circuit is enabled)			$t_{d(E-A)}$	—	—	600	µs	Figure 6.47, Figure 6.48
LVDBAT operation stabilization time (when the VCC and VBAT_EHC pins are connected)			$t_{d(E-A)}$	—	—	600	µs	
LVDBAT operation stabilization time (when the VCC and VBAT_EHC pins are not connected)			$t_{d(E-A)}$	—	—	1000	µs	
Hysteresis width (LVD1)			V_{LVH}*2	—	60	—	mV	
Hysteresis width (LVD1)			V_{LVH}*3	—	55	—	mV	
Hysteresis width (LVD1)			V_{LVH}*4	—	50	—	mV	
Hysteresis width (LVD1)			V_{LVH}*5	—	45	—	mV	
Hysteresis width (LVD1)			V_{LVH}*6	—	40	—	mV	
Hysteresis width (LVD1)			V_{LVH}*7	—	35	—	mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the lowest value among voltage detection levels V_{POR}, V_{det1}, and V_{detBAT} for the power-on reset circuit and low-voltage detection circuit.
Note 2. When V_{det1_0} is selected.
Note 3. When V_{det1_1} and V_{det1_3} are selected.
Note 4. When V_{det1_5} is selected.
Note 5. When V_{det1_7} is selected.
Note 6. When V_{det1_9} and V_{det1_B} are selected.
Note 7. When V_{det1_D} is selected.

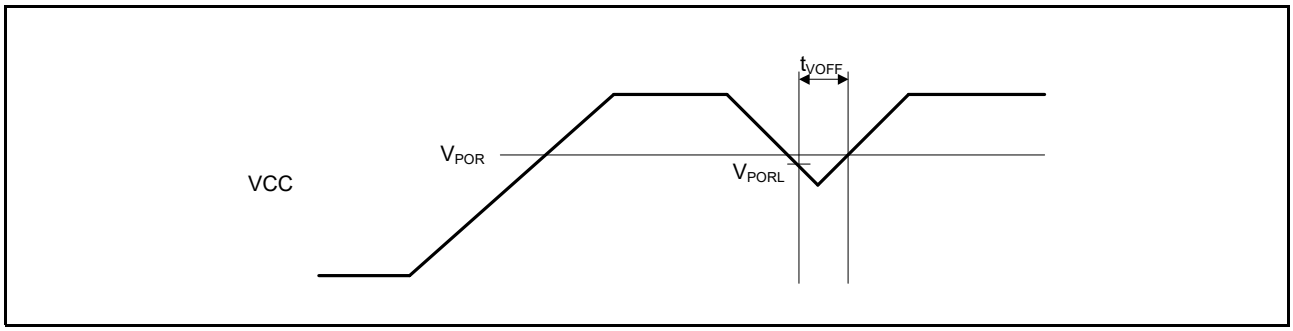


Figure 6.45 Power-on Reset Timing

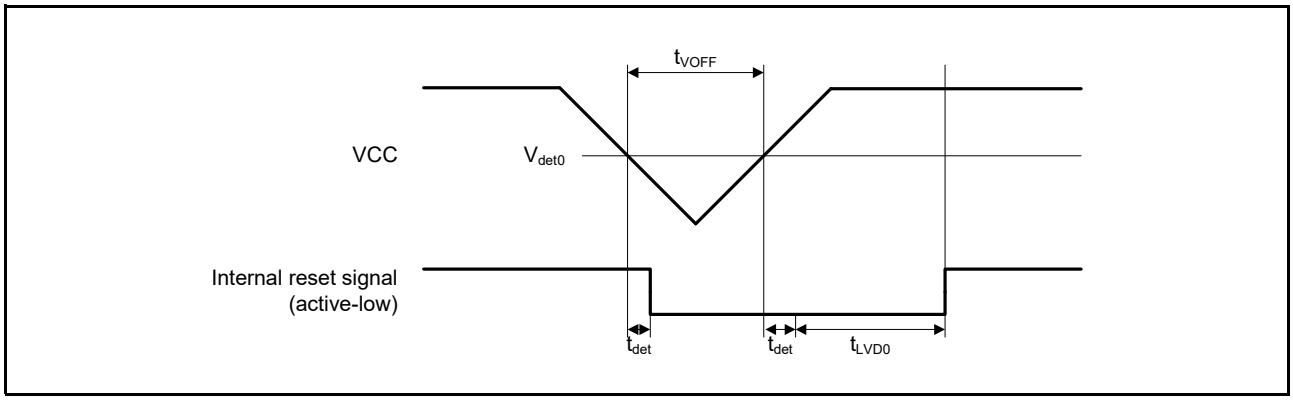


Figure 6.46 Timing of Voltage Detection by Voltage Monitoring Circuit 0 (V_{det0})

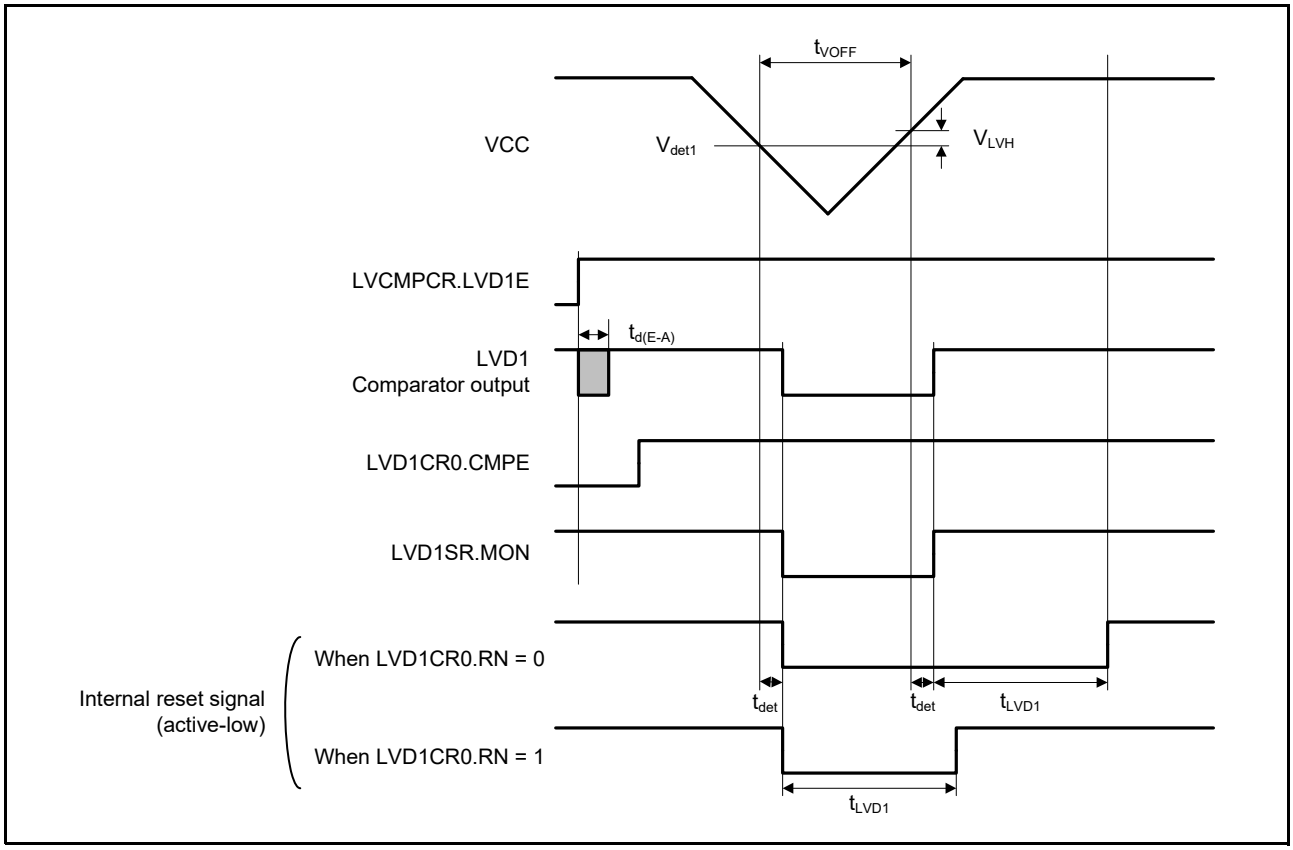


Figure 6.47 Timing of Voltage Detection by Voltage Monitoring Circuit 1 (V_{det1})

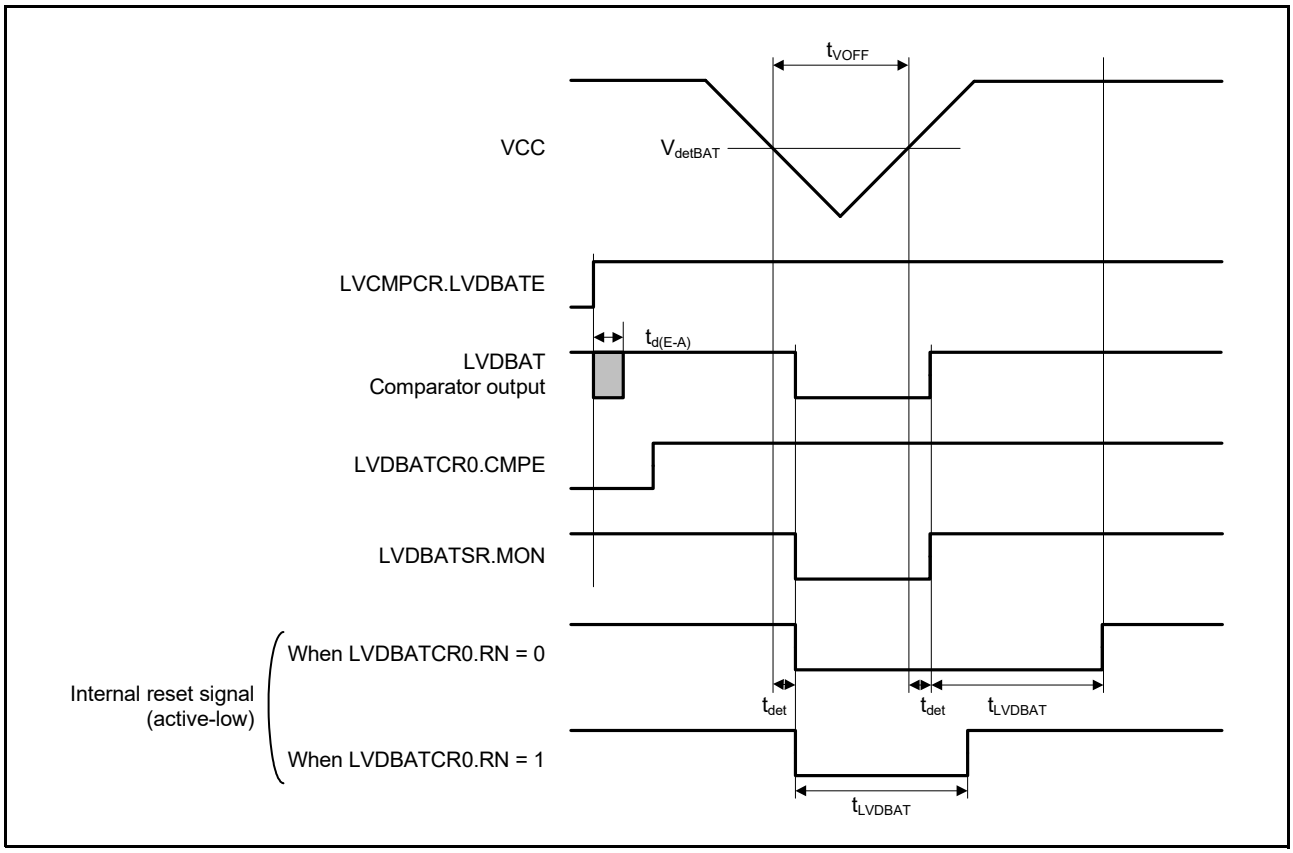


Figure 6.48 Timing of Voltage Detection by Voltage Monitoring BAT Circuit (V_{detBAT})

6.9 EHC Characteristics

Table 6.40 EHC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Current during reset	I_{CCEHC}	—	0.02	—	µA	VCC = VSC_VCC = 0 V, VCC_SU = VBAT_EHC = 2.5 V T_a = 25°C
Capacitance of the storage capacitor connected to VCC_SU*1, *3	C_{VCCSU}	—	100	—	µF	EHMD = 1 T_a = –40 to 60°C
		—	47	—		EHMD = 0 T_a = –40 to 50°C
		—	150	—		EHMD = 1 T_a = –40 to 85°C
Capacitance of the smoothing capacitor connected to VCC*1	C_{VCC}	—	10	—		T_a = –40 to 85°C
Current that can flow from VSC_VCC into LSI chip (when the secondary battery of 2.6 V is used)	I_{SC}	—	—	10	mA	VSC_VCC ≤ 3.6 V
Current that can flow from VSC_VCC into LSI chip (when the secondary battery of 3.0 V is used)		—	—	6	mA	VSC_VCC ≤ 3.6 V
Current that can flow from VBAT_EHC to IOVCCn*2	I_{VBAT}	—	—	30	mA	—
Current that can flow from VCC/IOVCC to IOVCCn*2	I_{VCC}	—	—	30	mA	—
Permissible value of output impedance on the VBAT_EHC side	R_{VBAT}	—	—	10	Ω	VSC_VCC ≤ 3.6 V
VBAT threshold voltage for secondary battery overcharging protection (when a 2.6-V secondary battery is in use)	VBAT_CHG	2.535	2.585	2.635	V	I_{SC} = 3 µA to 10 mA, VSC_VCC = VBAT_EHC
VBAT threshold voltage for secondary battery overcharging protection (when a 3.0-V secondary battery is in use)	VBAT_CHG	2.925	2.975	3.025	V	I_{SC} = 3 µA to 6 mA, VSC_VCC = VBAT_EHC
VCC threshold voltage for secondary battery overcharging protection	VCC_CHG	2.925	2.975	3.025	V	I_{SC} = 3 µA to 10 mA, VSC_VCC = VCC
High threshold voltage in high-speed activation of the LSI chip by using EHC capacitor charging (when a 2.6-V secondary voltage is in use)	VCC_SU_H	—	2.62	—	V	Value at VCC rise when VSC_VCC = VCC
Low threshold voltage in high-speed activation of the LSI chip by using EHC capacitor charging (when a 2.6-V secondary voltage is in use)	VCC_SU_L	—	2.32	—	V	Value at VCC fall when VSC_VCC = VCC
High threshold voltage in high-speed activation of the LSI chip by using EHC capacitor charging (when a 3.0-V secondary voltage is in use)	VCC_SU_H	—	2.83	—	V	Value at VCC rise when VSC_VCC = VCC
Low threshold voltage in high-speed activation of the LSI chip by using EHC capacitor charging (when a 3.0-V secondary voltage is in use)	VCC_SU_L	—	2.51	—	V	Value at VCC fall when VSC_VCC = VCC
Threshold voltage in activation of the LSI chip in the energy harvesting mode	VCC_SU_H	—	2.62	—	V	I_{SC} = 3 µA to 10 mA
Threshold voltage for the power generating element status flag	V_{ENOUT}	—	0.5	—	V	VCC_SU = 2.5 V
Minimum activating current required in energy harvesting startup mode	I_{SC}	—	3	—	µA	Ta = 25°C, VCC_SU and VCC are connected to 100-µF and 10-µF capacitors, respectively.

Note 1. See Figure 13.1 in the User's Manual: Hardware.
Note 2. IOVCCn refers to IOVCC0, IOVCC1, IOVCC2, and IOVCC3.
Note 3. Figure 6.50 shows the relation between the upper limit on temperature and the capacitance of the storage capacitor connected to VCC_SU. When the capacitance becomes insufficient for the temperature at which the capacitor is to be used, an activation current is required shown in Figure 6.51.

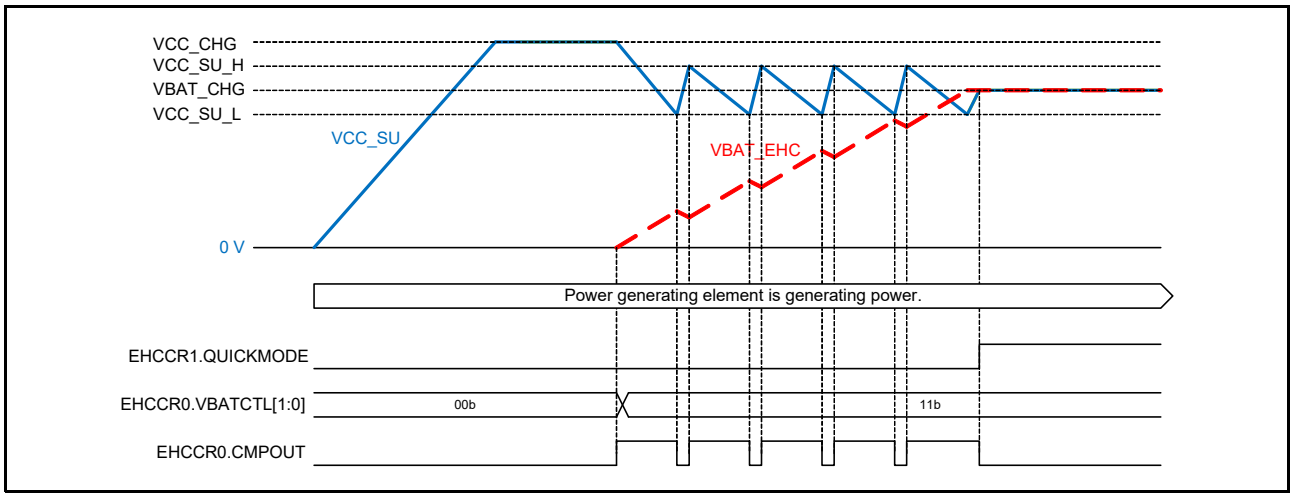


Figure 6.49 Charging Operations for the VBAT_EHC Pin in High-speed Activation of the LSI chip by Using EHC Capacitor Charging

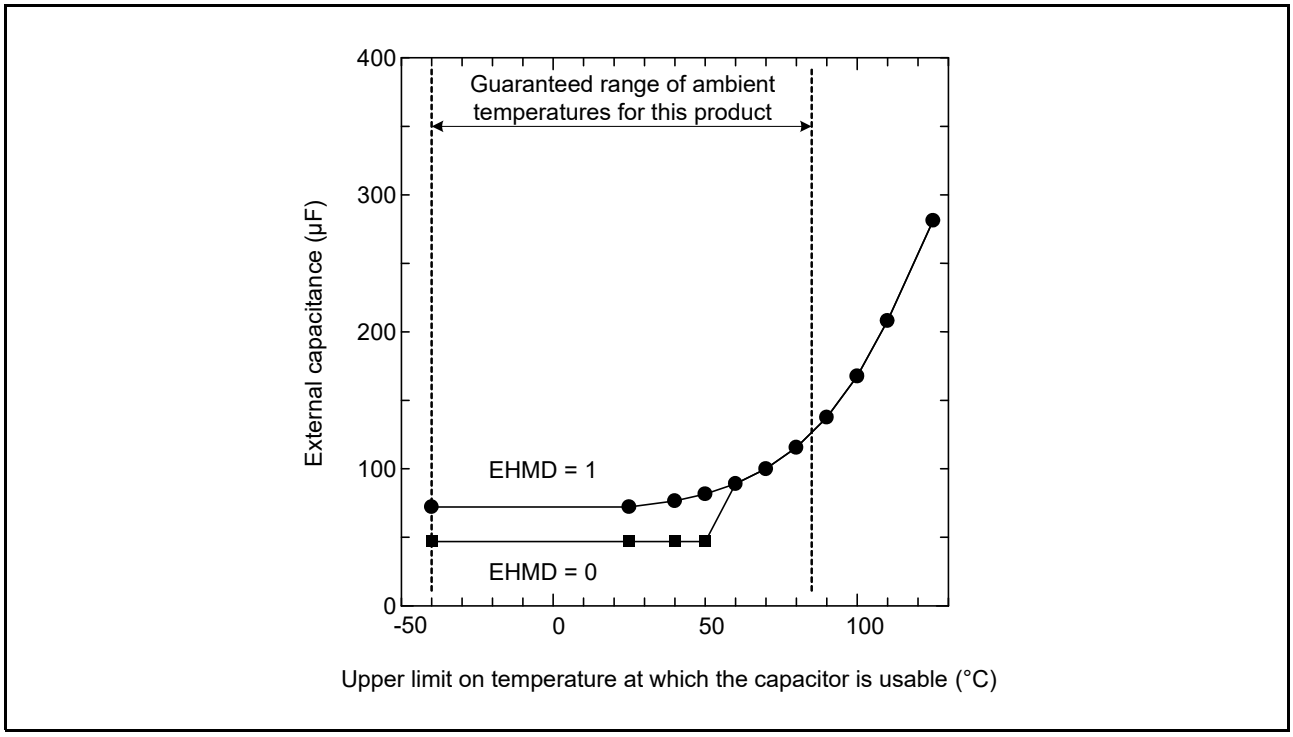


Figure 6.50 Relation between the Upper Limit on Temperature and Capacitance of the Storage Capacitor Connected to VCC_SU

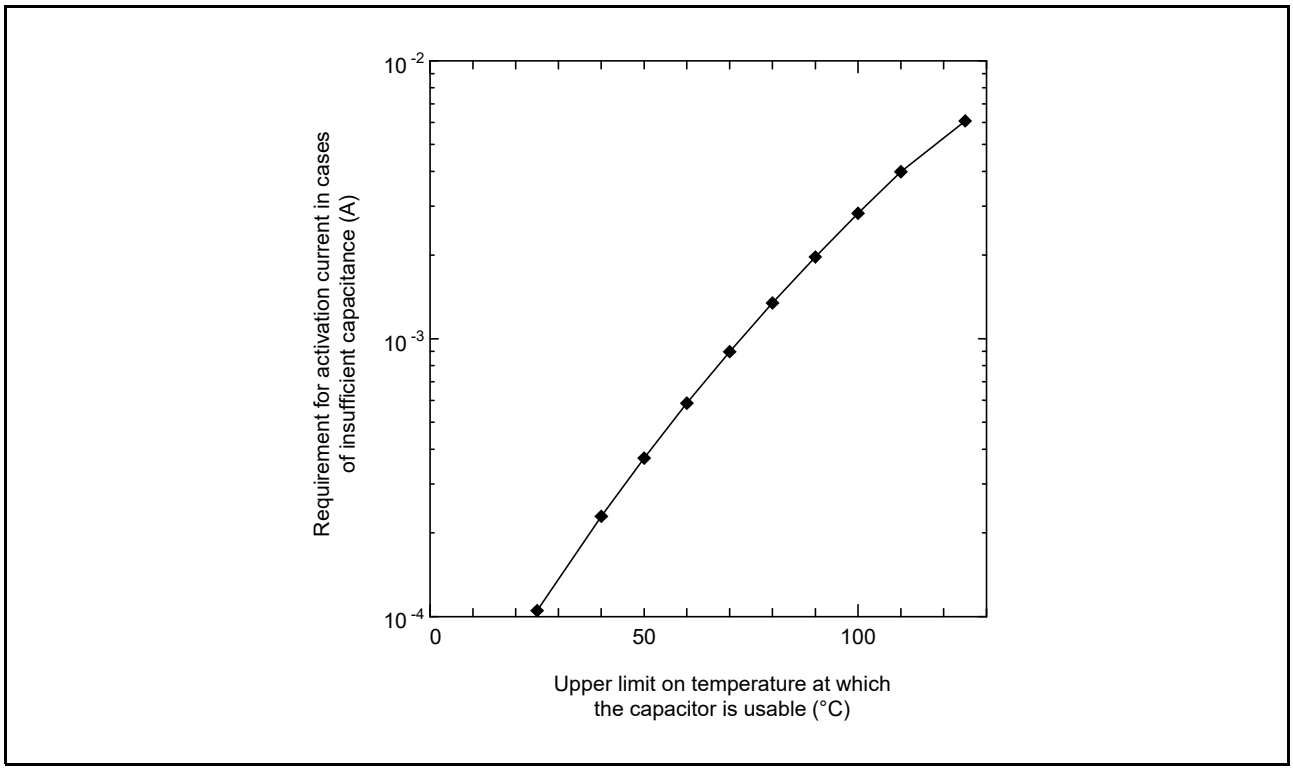


Figure 6.51 Relation between the Upper Limit of a Temperature and an Activation Current in the Case where Capacitance is Insufficient

6.10 Back Bias Voltage Control (VBBC) Circuit Characteristics

Table 6.41 VBBC Initial Setup Time

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
VBBC initial setup time*1	$t_{VBBSTUP}$	—	300*2	600*2, *3	ms	Figure 6.52
Internal voltage discharge time	t_{VBBDIS}	1	—	—	ms	Figure 6.53

Note 1. This is the time period between when 1 is written to VBBCR.VBBEN and when VBBST.VBBSTUP is changed to 1.
Note 2. This is the time when the value of the smoothing capacitor connected between the VBP and VBN pins is 1.0 F ± 20%.
Note 3. We do not inspect the characteristics of the back-bias voltage control circuit before shipment. The values presented in this manual are only for reference.

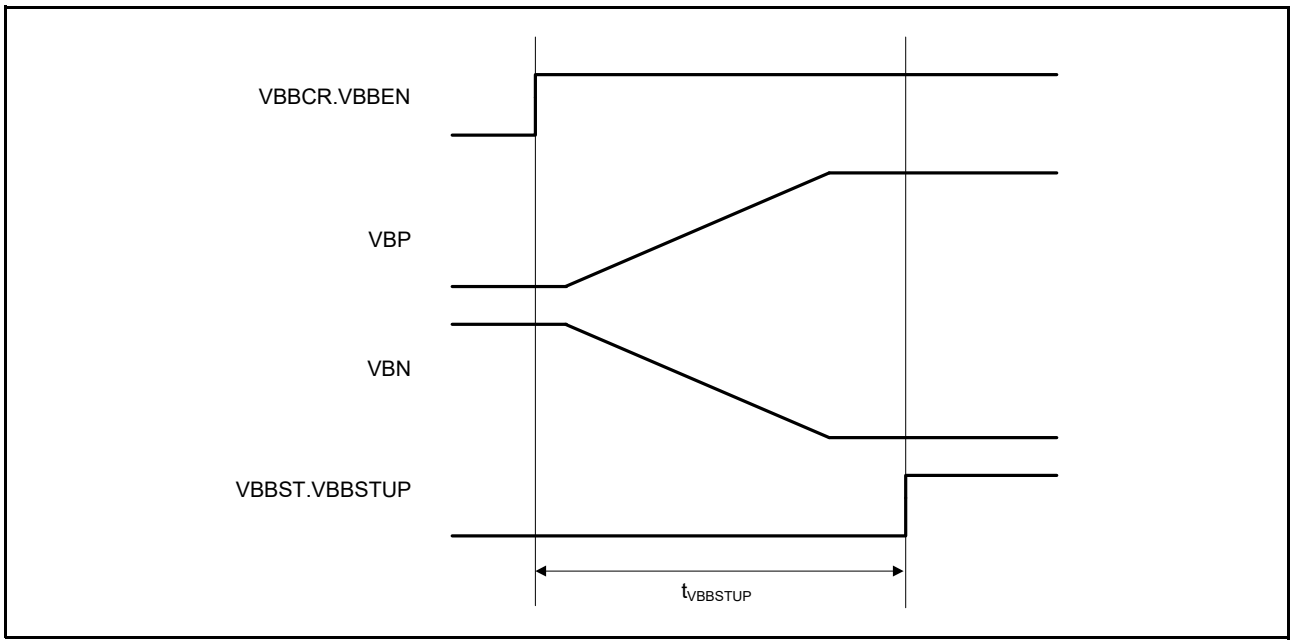


Figure 6.52 VBBC Initial Setup Timing

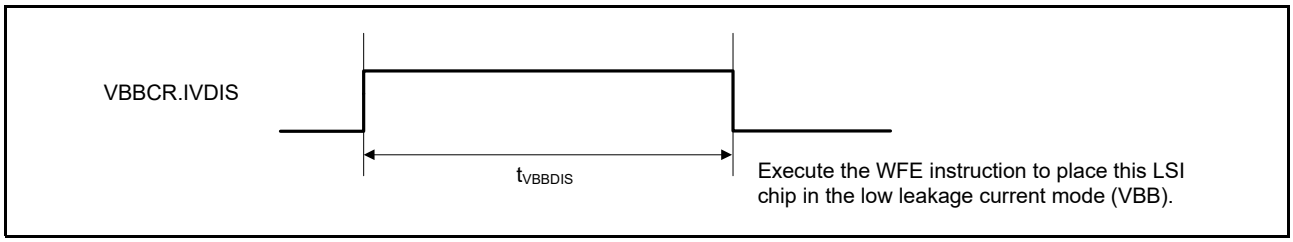


Figure 6.53 Internal Voltage Discharge Time

6.11 Flash Memory Characteristics

6.11.1 Code Flash Memory Characteristics

Table 6.42 Code Flash Memory Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Cycles of reprogramming and erasure*1		N_{PEC}	10000	—	—	Times	Tested in accord with the conditions defined by JEDEC
Data retention time		t_{DRP}	10	—	—	Year	

Note 1. The number of cycles of reprogramming and erasure defines the number of times a block can be erased. When the number of cycles of reprogramming and erasure is n, a block can be erased n times. For instance, if 8 bytes of data are written to the 256 different addresses on 8-byte boundaries within a 2-Kbyte block, erasing the whole block is counted as a single cycle of reprogramming and erasure. Note that programming of the same address is only allowed once; that is, overwriting is prohibited.

Table 6.43 Code Flash Memory Characteristics (2)

Item		Symbol	ICLK = 1 MHz			ICLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	8 bytes	t_{P8}	—	5.0	6.0	—	5.0	6.0	ms
	256 bytes	t_{P256}	—	5.0	6.0	—	5.0	6.0	ms
Erasure time	4 Kbytes	t_{E4K}	—	10.0	12.0	—	10.0	12.0	ms
Delay until first suspension during programming		t_{SPD1}	—	—	0.2	—	—	0.1	ms
Delay after second suspension during programming		t_{SPD2}	—	—	2.4	—	—	2.0	ms
Delay until first suspension during erasure		t_{SED1}	—	—	0.2	—	—	0.1	ms
Delay after second suspension during erasure		t_{SED2}	—	—	2.4	—	—	2.0	ms
Forced stop command		t_{FD}	—		0.2	—	—	0.1	ms

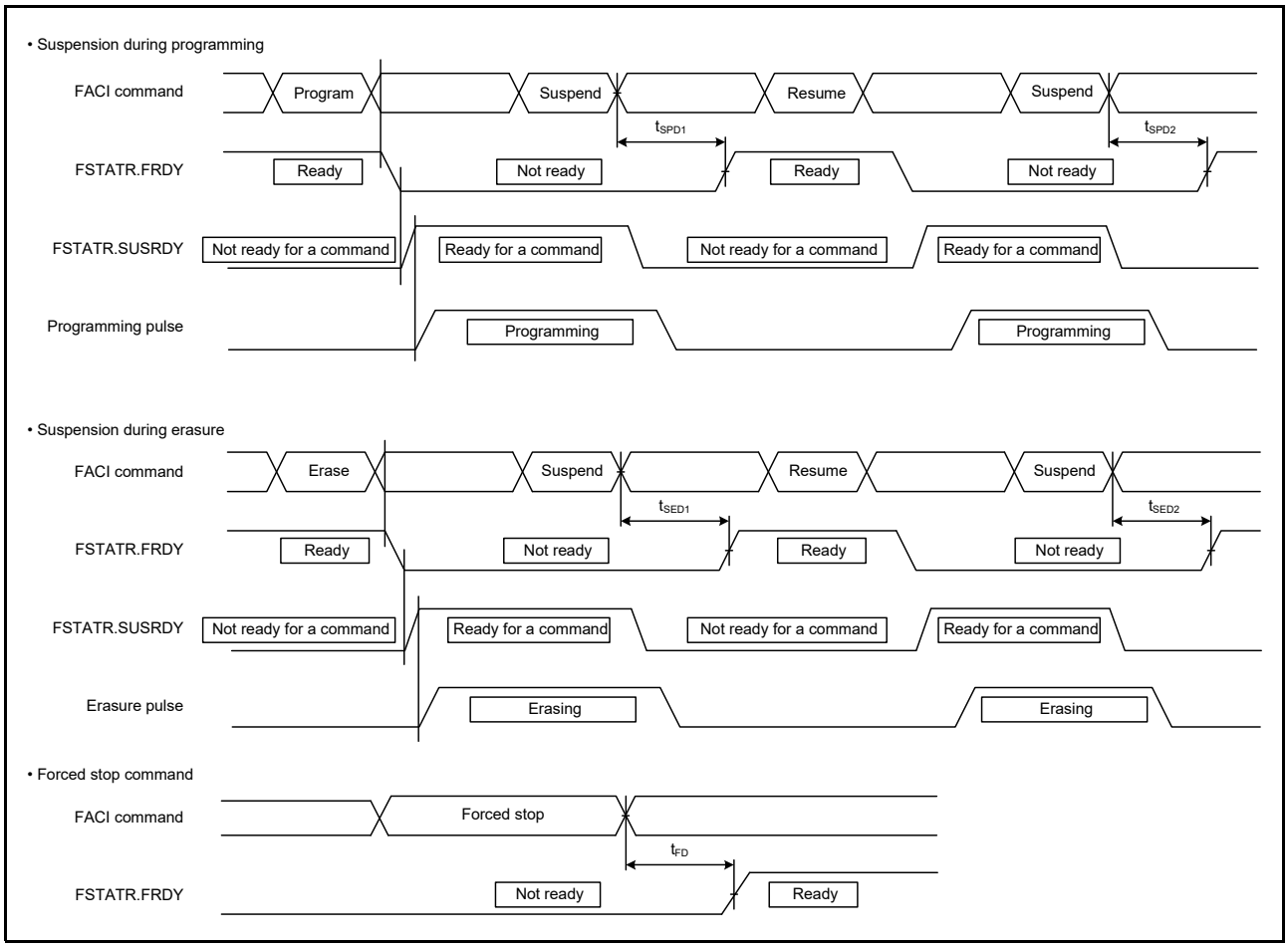


Figure 6.54 Timing of Suspension during Programming and Erasure and Timing of Forced Stop of the Flash Memory

6.12 BLE Characteristics

6.12.1 Transmission Characteristics

Table 6.44 Transmission Characteristics
Conditions: VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Range of frequency	RF_{CF}	2402	—	2480	MHz	
Data rate	RF_{DATA_2M}	—	2	—	Mbps	
	RF_{DATA_1M}	—	1	—	Mbps	
	RF_{DATA_500k}	—	500	—	kbps	
	RF_{DATA_125k}	—	125	—	kbps	
Maximum transmitted output power	RF_{POWER}	—	0	2	dBm	0 dBm output mode
		—	4	6	dBm	4 dBm output mode
Output frequency error	RF_{TXFERR}	–10	—	10	ppm	*1

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.
Note 1. This does not take frequency errors due to manufacturing irregularities, drift with temperature, or deterioration of the crystal over time into account.

6.12.2 Reception Characteristics (2 Mbps)

Table 6.45 Reception Characteristics
Conditions: VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Input frequency	RF_{RXFIN_2M}	2402	—	2480	MHz		
Maximum input level	RF_{LEVL_2M}	–10	4	—	dBm	*1	
Receiver sensitivity	RF_{STY_2M}	—	–92	—	dBm	*1	
Secondary emission strength	RF_{RXSP_2M}	—	–72	–57	dBm	30 MHz to 1 GHz	
		—	–54	–47	dBm	1 GHz to 12 GHz	
Co-channel rejection ratio	RF_{CCR_2M}	—	–8	—	dB	Prf = –67 dBm*1	
Adjacent channel rejection ratio	RF_{ADCR_2M}	—	2	—	dB	Prf = –67 dBm*1	±2 MHz
		—	35	—	dB		±4 MHz
		—	39	—	dB		±6 MHz
Blocking	RF_{BLK_2M}	—	–1	—	dBm	Prf = –67 dBm*1	30 MHz to 2000 MHz
		—	–25	—	dBm		2000 MHz to 2399 MHz
		—	–21	—	dBm		2484 MHz to 3000 MHz
		—	–10	—	dBm		> 3000 MHz
Allowable frequency deviation*2	RF_{RXFER_2M}	–120	—	120	ppm	*1	
RSSI accuracy	RF_{RSSIS_2M}	—	±4	—	dB	–70 dBm ≤ Prf ≤ –10 dBm	

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.
Note 1. PER ≤ 30.8%, and a 37-byte payload
Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip

6.12.3 Reception Characteristics (1 Mbps)

Table 6.46 Reception Characteristics
Conditions: VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Input frequency	RF_{RXFIN_1M}	2402	—	2480	MHz		
Maximum input level	RF_{LEVL_1M}	–10	4	—	dBm	*1	
Receiver sensitivity	RF_{STY_1M}	—	–95	—	dBm	*1	
Secondary emission strength	RF_{RXSP_1M}	—	–72	–57	dBm	30 MHz to 1 GHz	
		—	–54	–47	dBm	1 GHz to 12 GHz	
Co-channel rejection ratio	RF_{CCR_1M}	—	–7	—	dB	Prf = –67 dBm*1	
Adjacent channel rejection ratio	RF_{ADCR_1M}	—	–1	—	dB	Prf = –67 dBm*1	±1 MHz
		—	34	—	dB		±2 MHz
		—	35	—	dB		±3 MHz
Blocking	RF_{BLK_1M}	—	0	—	dBm	Prf = –67 dBm*1	30 MHz to 2000 MHz
		—	–24	—	dBm		2000 MHz to 2399 MHz
		—	–20	—	dBm		2484 MHz to 3000 MHz
		—	–4	—	dBm		> 3000 MHz
Allowable frequency deviation*2	RF_{RXFER_1M}	–120	—	120	ppm	*1	
RSSI accuracy	RF_{RSSIS_1M}	—	±4	—	dB	–70 dBm ≤ Prf ≤ –10 dBm	

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.
Note 1. PER ≤ 30.8%, and a 37-byte payload
Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip

6.12.4 Reception Characteristics (500 kbps)

Table 6.47 Reception Characteristics
Conditions: VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Input frequency	RF_{RXFIN_500k}	2402	—	2480	MHz		
Maximum input level	RF_{LEVL_500k}	–10	4	—	dBm	*1	
Receiver sensitivity	RF_{STY_500k}	—	–100	—	dBm	*1	
Secondary emission strength	RF_{RXSP_500k}	—	–72	–57	dBm	30 MHz to 1 GHz	
		—	–54	–47	dBm	1 GHz to 12 GHz	
Co-channel rejection ratio	RF_{CCR_500k}	—	–4	—	dB	Prf = –72 dBm*1	
Adjacent channel rejection ratio	RF_{ADCR_500k}	—	6	—	dB	Prf = –72 dBm*1	±1 MHz
		—	36	—	dB		±2 MHz
		—	42	—	dB		±3 MHz
Blocking	RF_{BLK_500k}	—	0	—	dBm	Prf = –72 dBm*1	30 MHz to 2000 MHz
		—	–23	—	dBm		2000 MHz to 2399 MHz
		—	–20	—	dBm		2484 MHz to 3000 MHz
		—	–7	—	dBm		> 3000 MHz
Allowable frequency deviation*2	RF_{RXFER_500k}	–120	—	120	ppm	*1	
RSSI accuracy	RF_{RSSIS_500k}	—	±4	—	dB	–70 dBm ≤ Prf ≤ –10 dBm	

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.
Note 1. PER ≤ 30.8%, and a 37-byte payload
Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip

6.12.5 Reception Characteristics (125 kbps)

Table 6.48 Reception Characteristics
Conditions: VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Input frequency	RF_{RXFIN_125k}	2402	—	2480	MHz		
Maximum input level	RF_{LEVL_125k}	–10	4	—	dBm	*1	
Receiver sensitivity	RF_{STY_125k}	—	–105	—	dBm	*1	
Secondary emission strength	RF_{RXSP_125k}	—	–72	–57	dBm	30 MHz to 1 GHz	
		—	–54	–47	dBm	1 GHz to 12 GHz	
Co-channel rejection ratio	RF_{CCR_125k}	—	–2	—	dB	Prf = –79 dBm*1	
Adjacent channel rejection ratio	RF_{ADCR_125k}	—	12	—	dB	Prf = –79 dBm*1	±1 MHz
		—	39	—	dB		±2 MHz
		—	45	—	dB		±3 MHz
Blocking	RF_{BLK_125k}	—	0	—	dBm	Prf = –79 dBm*1	30 MHz to 2000 MHz
		—	–23	—	dBm		2000 MHz to 2399 MHz
		—	–20	—	dBm		2484 MHz to 3000 MHz
		—	–1	—	dBm		> 3000 MHz
Allowable frequency deviation*2	RF_{RXFER_125k}	–120	—	120	ppm	*1	
RSSI accuracy	RF_{RSSIS_125k}	—	±4	—	dB	T_a = +25°C, –70 dBm ≤ Prf ≤ –10 dBm	

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.
Note 1. PER ≤ 30.8%, and a 37-byte payload
Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip

6.13 Serial Wire Debug (SWD) Characteristics

Table 6.49 SWD Characteristics
Conditions: VCC = AVCC0 = 1.62 to 3.6 V

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NORMAL	SWCLK clock cycle time	$t_{SWCKcyc}$	80	—	—	ns	Figure 6.55
	SWCLK clock high-level pulse width	t_{SWCKH}	$t_{SWCKcyc} \times 0.5 - t_{SWCKr}$	—	—	ns	
	SWCLK clock low-level pulse width	t_{SWCKL}	$t_{SWCKcyc} \times 0.5 - t_{SWCKf}$	—	—	ns	
	SWCLK clock rise time	t_{SWCKr}	—	—	7	ns	
	SWCLK clock fall time	t_{SWCKf}	—	—	7	ns	
	SWDIO setup time	t_{SWDS}	$t_{SWCKcyc} \times 0.2$	—	—	ns	Figure 6.56
	SWDIO hold time	t_{SWDH}	$t_{SWCKcyc} \times 0.2$	—	—	ns	
	SWDIO data delay time	t_{SWDD}	2	—	50	ns	
VBB	SWCLK clock cycle time	$t_{SWCKcyc}$	30000	—	—	ns	Figure 6.55
	SWCLK clock high-level pulse width	t_{SWCKH}	$t_{SWCKcyc} \times 0.5 - t_{SWCKr}$	—	—	ns	
	SWCLK clock low-level pulse width	t_{SWCKL}	$t_{SWCKcyc} \times 0.5 - t_{SWCKf}$	—	—	ns	
	SWCLK clock rise time	t_{SWCKr}	—	—	7	ns	
	SWCLK clock fall time	t_{SWCKf}	—	—	7	ns	
	SWDIO setup time	t_{SWDS}	1000	—	—	ns	Figure 6.56
	SWDIO hold time	t_{SWDH}	1000	—	—	ns	
	SWDIO data delay time	t_{SWDD}	2	—	1000	ns	

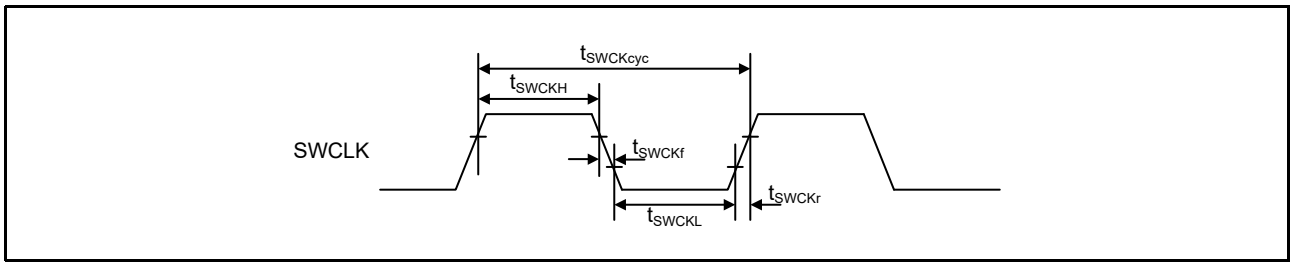


Figure 6.55 SWD SWCLK Timing

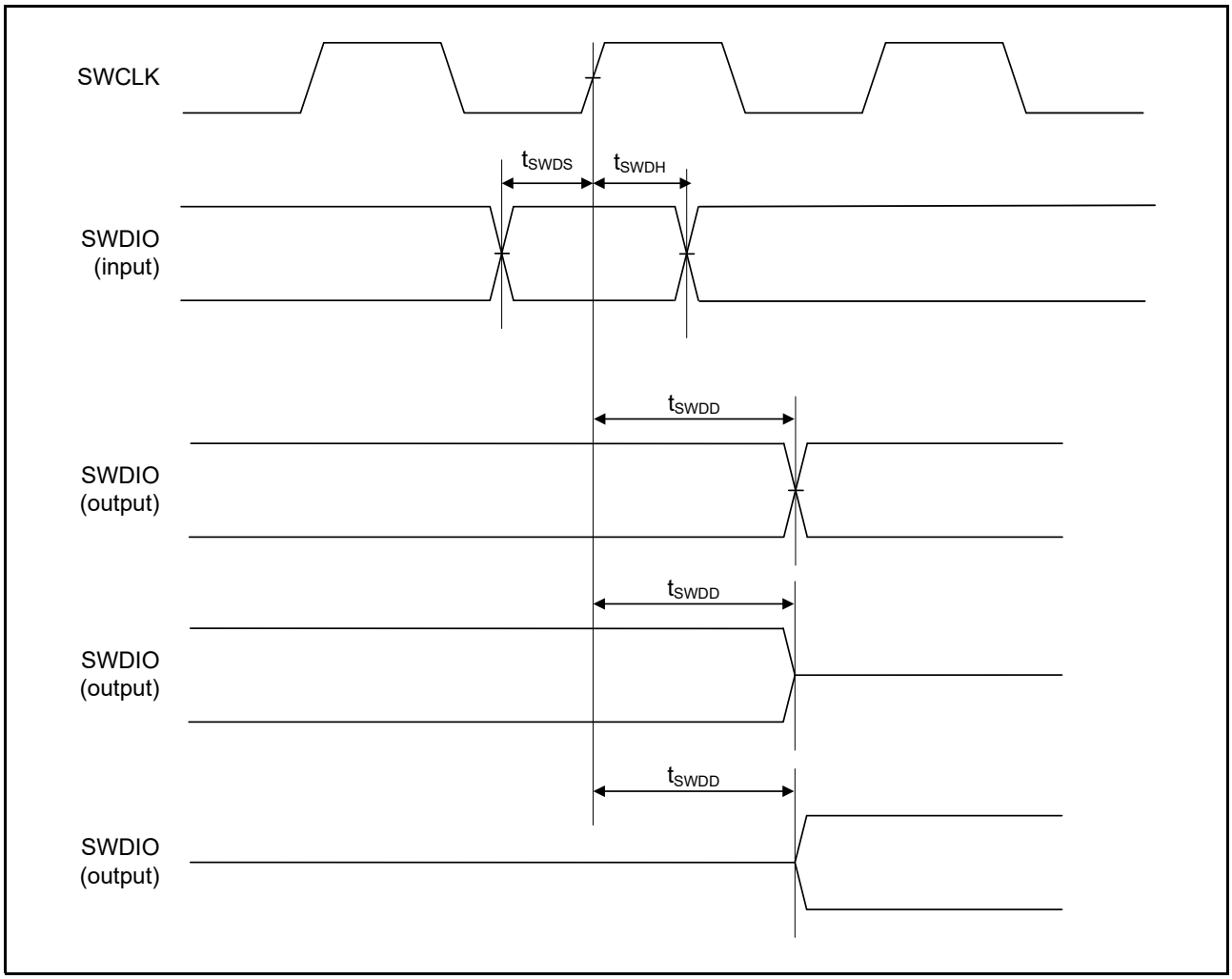
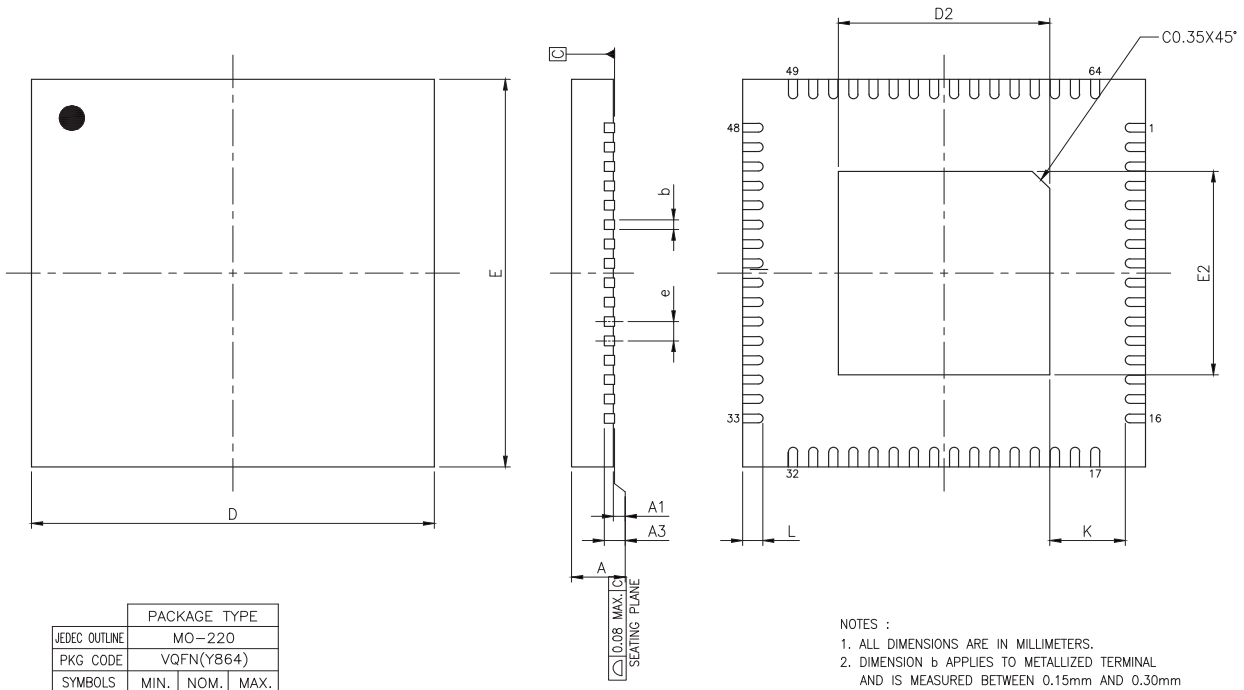


Figure 6.56 SWD Input and Output Timing

Appendix A. Package Dimensions

For the latest information on package dimensions and mounting, see “Packaging Information” on the Renesas website.

JEITA Package code	RENESAS code	MASS [Typ.]
P-VQFN64-8x8-0.40	PVQN0064LE-A	0.45



	PACKAGE TYPE		
JEDEC OUTLINE	MO−220		
PKG CODE	VQFN(Y864)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	8.00 BSC		
E	8.00 BSC		
e	0.40 BSC		
L	0.35	0.40	0.45
K	0.20	—	—

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
268X26* MIL	6.40	6.50	6.60	6.40	6.50	6.60	V	X	W(V)LLE−2

"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure A.1 64-Pin QFN (PVQN0064LE-A)

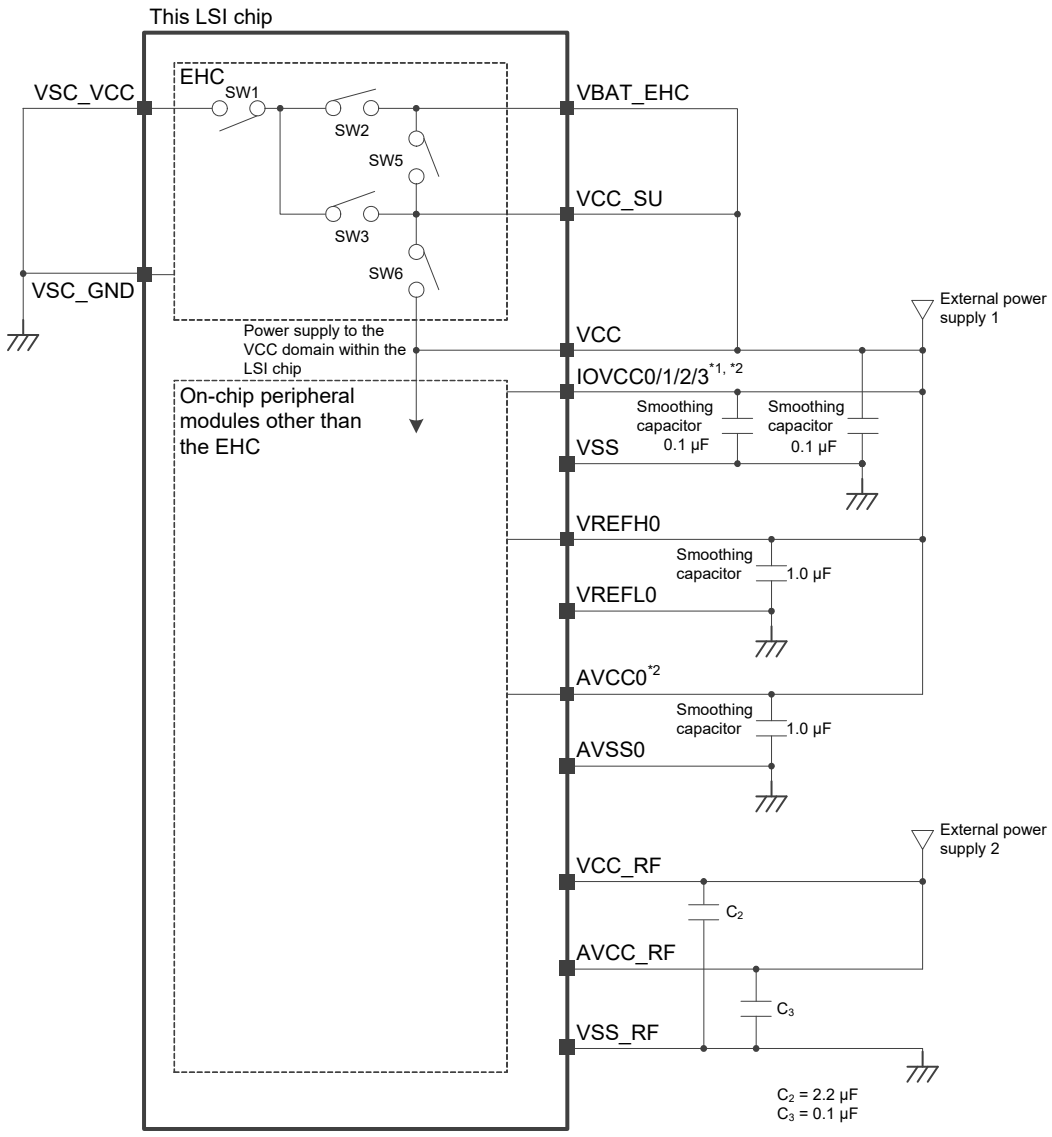
Appendix B. Connecting the Capacitors to the Power Supply Pins

The power supply pins must be connected to the ground via smoothing capacitors placed close to each of the power supply pins. This appendix shows representative examples of connections.

Setting the power supply open control register (VOCR) enables the external supply of power. In an environment where much external noise is present, place a 10-µF capacitor close to each of the power supply pins as required, as well as the capacitors in the relevant example, to improve robustness against external noise and obtain stable operation of the circuit. For more details, see Table 1.4 in section 1.5, Pin Functions of section 1, Overview.

B.1 Example of Connections for Normal Startup Mode

Figure B.1 shows an example of connections for normal startup mode with two external power sources and the EHC not in use.

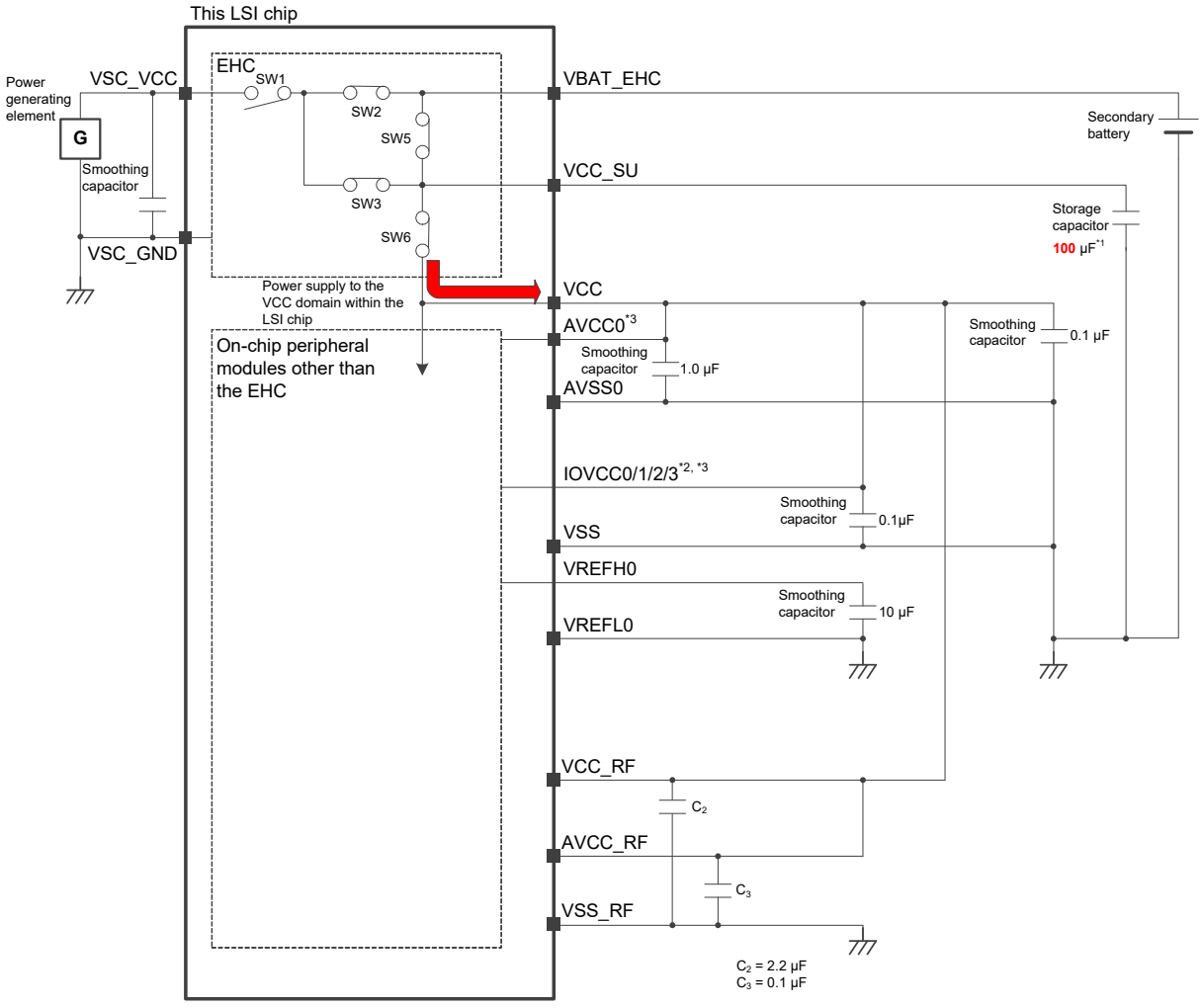


Note: For details on the connections and values of capacitors, see Table 1.4 in section 1.5, Pin Functions of section 1, Overview.
Note: For details on the BLE pins, see Guidelines to Designing the RE01B Bluetooth Board.
Note 1. A smoothing capacitor must be connected to each of IOVCC0, IOVCC1, IOVCC2, and IOVCC3.
Note 2. Set the VOCR register to enable the supply of power to these pins.

Figure B.1 Example of Connections for Normal Startup Mode

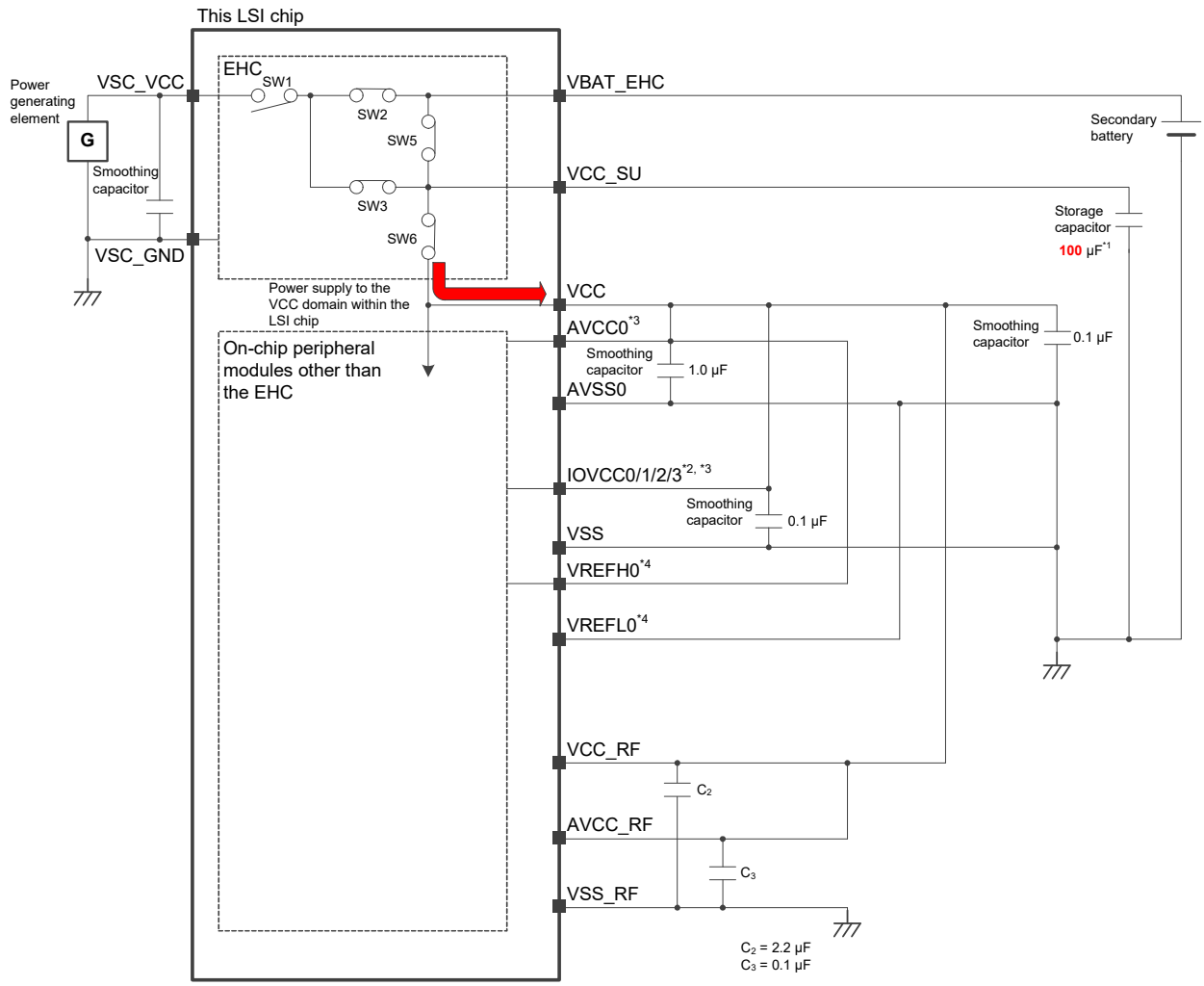
B.2 Example of Connections in Energy Harvesting Startup Mode (1)

Figure B.2 shows an example of connections in energy harvesting startup mode with the EHC and VREF in use, and no external power supplies. Figure B.3 shows an example where AVCC0 is the reference voltage.



Note: For details on the connections and values of capacitors, see Table 1.4 in section 1.5, Pin Functions of section 1, Overview.
Note: For details on the BLE pins, see Guidelines to Designing the RE01B Bluetooth Board.
Note 1. The required capacitance of the storage capacitor depends on the ambient temperature range. For details, see section 6.9, EHC Characteristics.
Note 2. A smoothing capacitor must be connected to each of IOVCC0, IOVCC1, IOVCC2, and IOVCC3.
Note 3. Set the VOCR register to enable the supply of power to these pins.

Figure B.2 Example of Connections in Energy Harvesting Startup Mode with the VREF in Use (1)

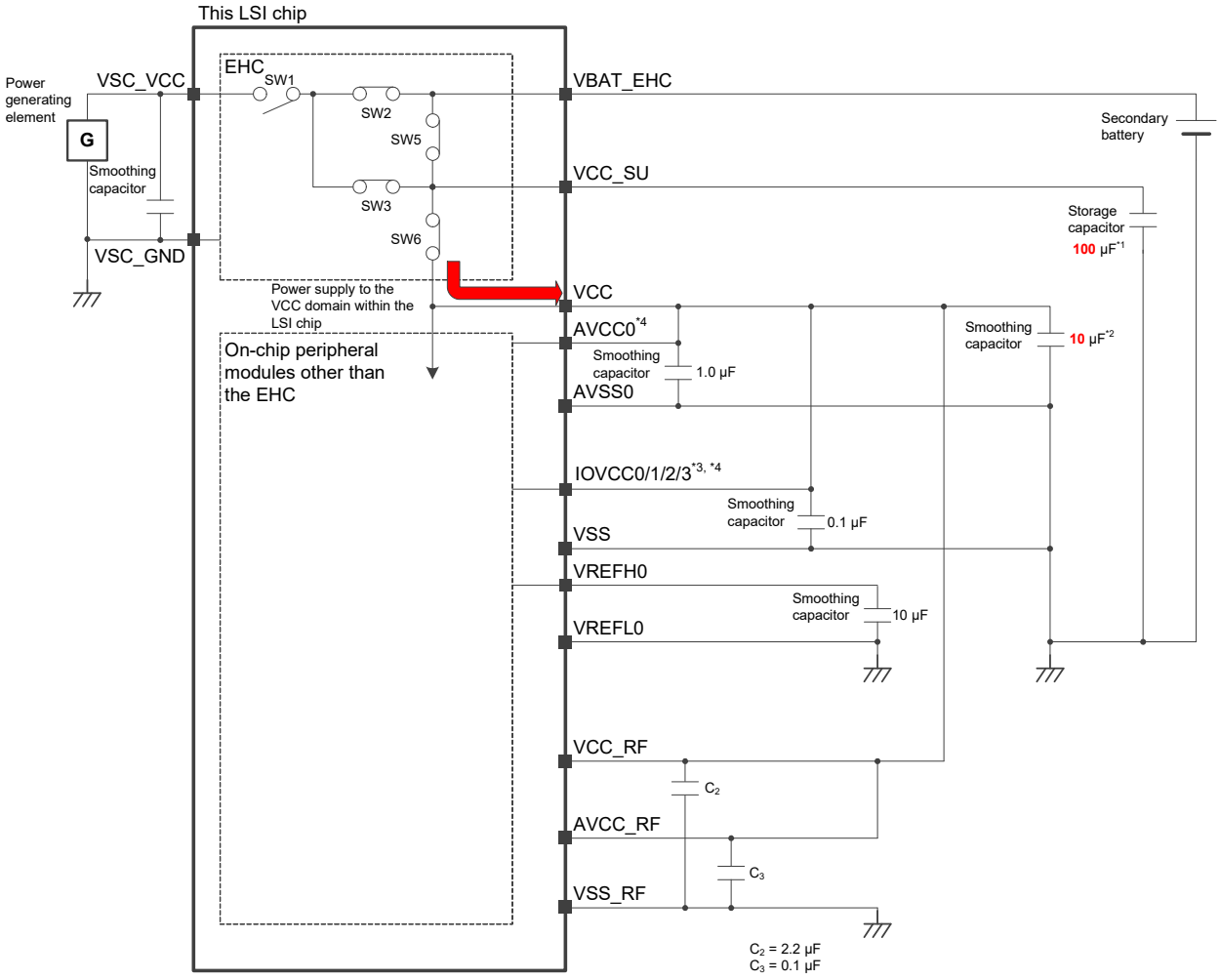


Note: For details on the connections and values of capacitors, see Table 1.4 in section 1.5, Pin Functions of section 1, Overview.
Note: For details on the BLE pins, see Guidelines to Designing the RE01B Bluetooth Board.
Note 1. The required capacitance of the storage capacitor depends on the ambient temperature range. For details, see section 6.9, EHC Characteristics.
Note 2. A smoothing capacitor must be connected to each of IOVCC0, IOVCC1, IOVCC2, and IOVCC3.
Note 3. Set the VOCR register to enable the supply of power to these pins.
Note 4. In this example, the setting of the ADHVREFCNT register in the S14AD is 00h (selecting AVCC0 as the reference voltage).

Figure B.3 Example of Connections in Energy Harvesting Startup Mode with AVCC0 as the Reference Voltage

B.3 Example of Connections in Energy Harvesting Startup Mode (2)

Figure B.4 shows an example of connections in energy harvesting startup mode with the EHC in use and no external power supplies.

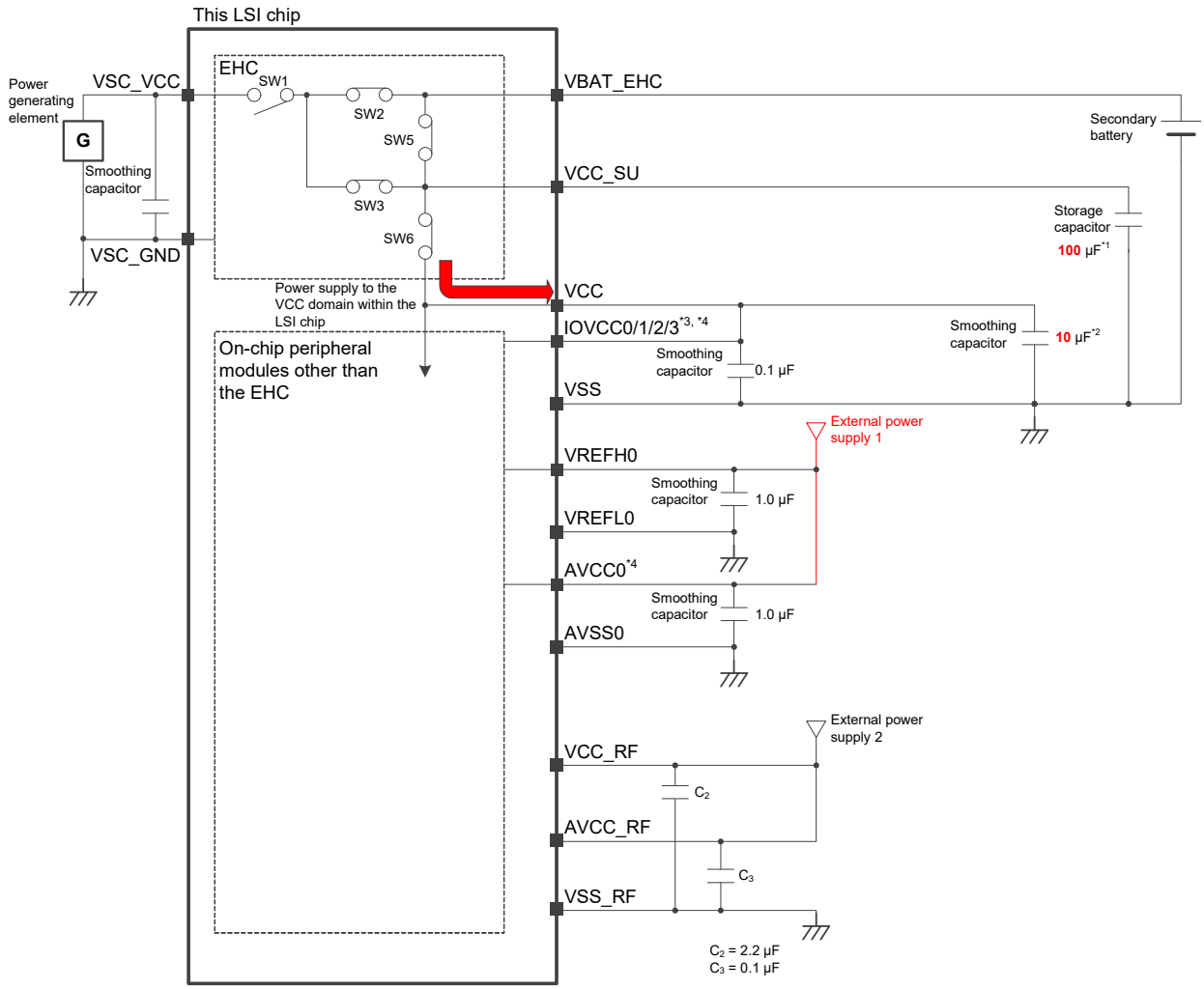


Note: For details on the connections and values of capacitors, see Table 1.4 in section 1.5, Pin Functions of section 1, Overview.
Note: For details on the BLE pins, see Guidelines to Designing the RE01B Bluetooth Board.
Note 1. The required capacitance of the storage capacitor depends on the ambient temperature range. For details, see section 6.9, EHC Characteristics.
Note 2. The capacitance must be at least 1/10 that of the storage capacitor connected to the VCC_SU pin.
Note 3. A smoothing capacitor must be connected to each of IOVCC0, IOVCC1, IOVCC2, and IOVCC3.
Note 4. Set the VOCR register to enable the supply of power to these pins.

Figure B.4 Example of Connections in Energy Harvesting Startup Mode with the VREF in Use (2)

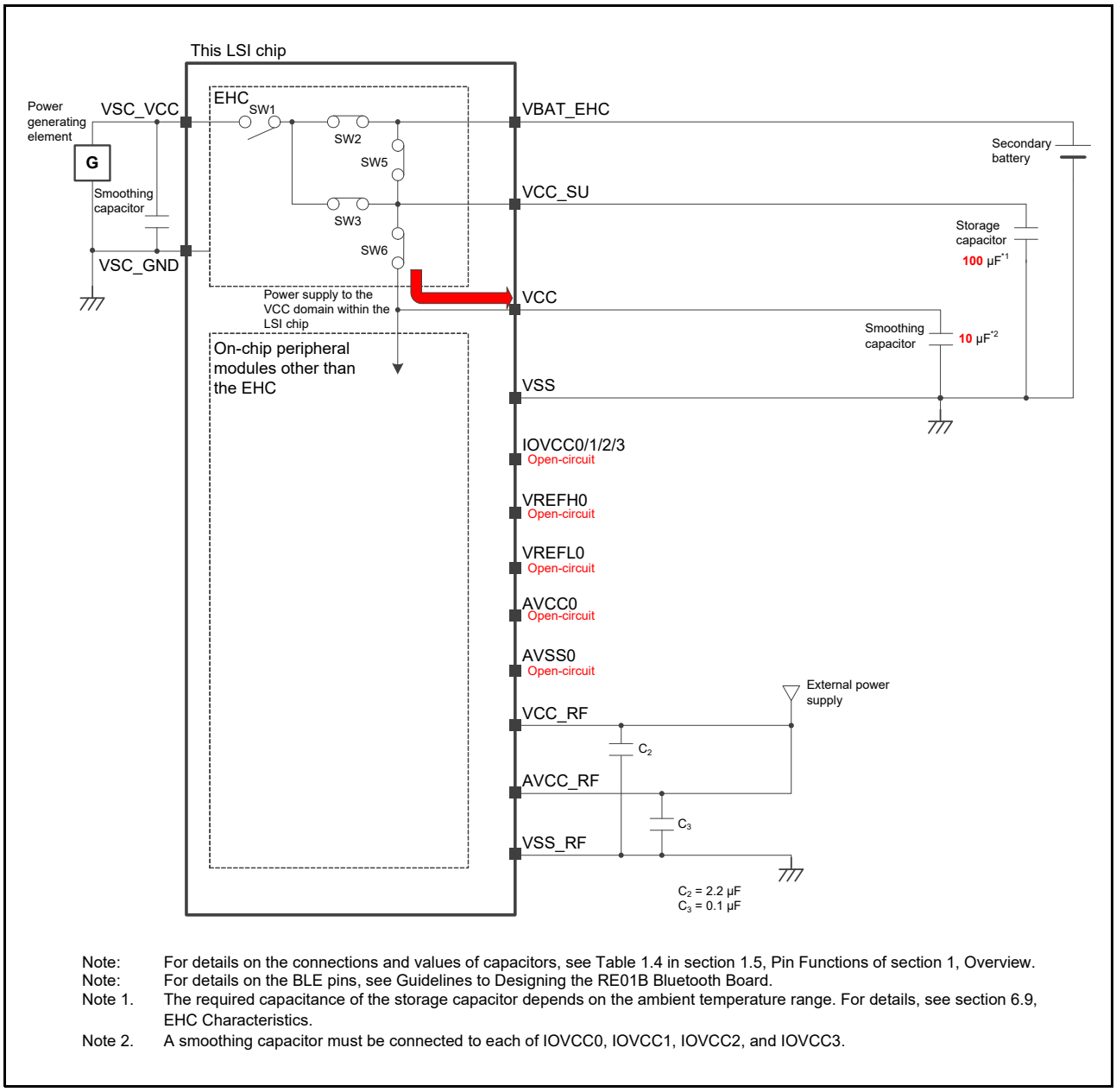
B.4 Example of Connections in Energy Harvesting Startup Mode (3)

Figure B.5 shows an example of connections in energy harvesting startup mode with the EHC in use and separate power sources for the analog circuits and RF circuit. Figure B.6 shows an example with no analog circuits in use.



Note: For details on the connections and values of capacitors, see Table 1.4 in section 1.5, Pin Functions of section 1, Overview.
Note: For details on the BLE pins, see Guidelines to Designing the RE01B Bluetooth Board.
Note 1. The required capacitance of the storage capacitor depends on the ambient temperature range. For details, see section 6.9, EHC Characteristics.
Note 2. The capacitance must be at least 1/10 that of the storage capacitor connected to the VCC_SU pin.
Note 3. A smoothing capacitor must be connected to each of IOVCC0, IOVCC1, IOVCC2, and IOVCC3.
Note 4. Set the VOCR register to enable the supply of power to these pins.

Figure B.5 Example of Connections in Energy Harvesting Startup Mode with Certain External Power Sources



Note: For details on the connections and values of capacitors, see Table 1.4 in section 1.5, Pin Functions of section 1, Overview.
Note: For details on the BLE pins, see Guidelines to Designing the RE01B Bluetooth Board.
Note 1. The required capacitance of the storage capacitor depends on the ambient temperature range. For details, see section 6.9, EHC Characteristics.
Note 2. A smoothing capacitor must be connected to each of IOVCC0, IOVCC1, IOVCC2, and IOVCC3.

Figure B.6 Example of Minimum Connections in Energy Harvesting Startup Mode

REVISION HISTORY	RE01B Group Product with 1.5-Mbyte Flash Memory Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Oct 07, 2020	—	First edition, issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Renesas Electronics Corporation
TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan

Renesas Electronics America Inc. Milpitas Campus
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics America Inc. San Jose Campus
6024 Silver Creek Valley Road, San Jose, CA 95138, USA
Tel: +1-408-284-8200, Fax: +1-408-284-2775

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 101-T01, Floor 1, Building 7, Yard No. 7, 8th Street, Shangdi, Haidian District, Beijing 100085, China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai 200333, China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, #06-02 Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit No 3A-1 Level 3A Tower 8 UOA Business Park, No 1 Jalan Pengaturcara U1/51A, Seksyen U1, 40150 Shah Alam, Selangor, Malaysia
Tel: +60-3-5022-1288, Fax: +60-3-5022-1290

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

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