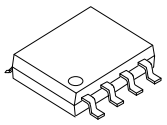
HIGH PRECISION LOW COST MCM POWER SWITCH



SOP-8

■ DESCRIPTION

The UTC **US2351** is a high performance, high precision and low cost PWM Power switch for non-isolated buck application. It combines a dedicated current mode PWM controller and error amplifier for low component count. UTC **US2351** use UTC proprietary frequency shuffling technique for EMI performance. And oscillator with frequency-reduction control is implemented.

The UTC **US2351** has soft start control and protection function, such as Cycle-by-Cycle current limiting, Over Loading Protection, Output Short-Circuit Protection, R_{CS} short Protection, OTP, V_{DD} OVP, and UVLO.

■ FEATURES

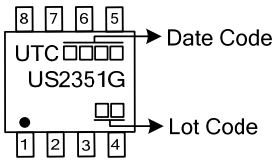
* Power on soft-start
* Load compensation
* Built-in error amplifier
* Oscillator of fixed frequency with frequency-reduction control
* Frequency shuffling for EMI improvement
* Built-in Leading Edge Blanking (LEB)
* Cycle-by-Cycle current limiting
* Over loading protection
* Output short-circuit protection
* V_{DD} Under Voltage Lockout with hysteresis (UVLO)
* V_{DD} OVP

■ ORDERING INFORMATION

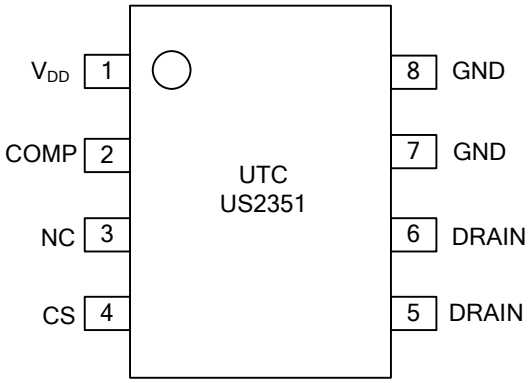
Ordering Number	Package	Packing
US2351G-S08-R	SOP-8	Tape Reel

US2351G-S08-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) S08: SOP-8 (3) G: Halogen Free and Lead Free

■ MARKING



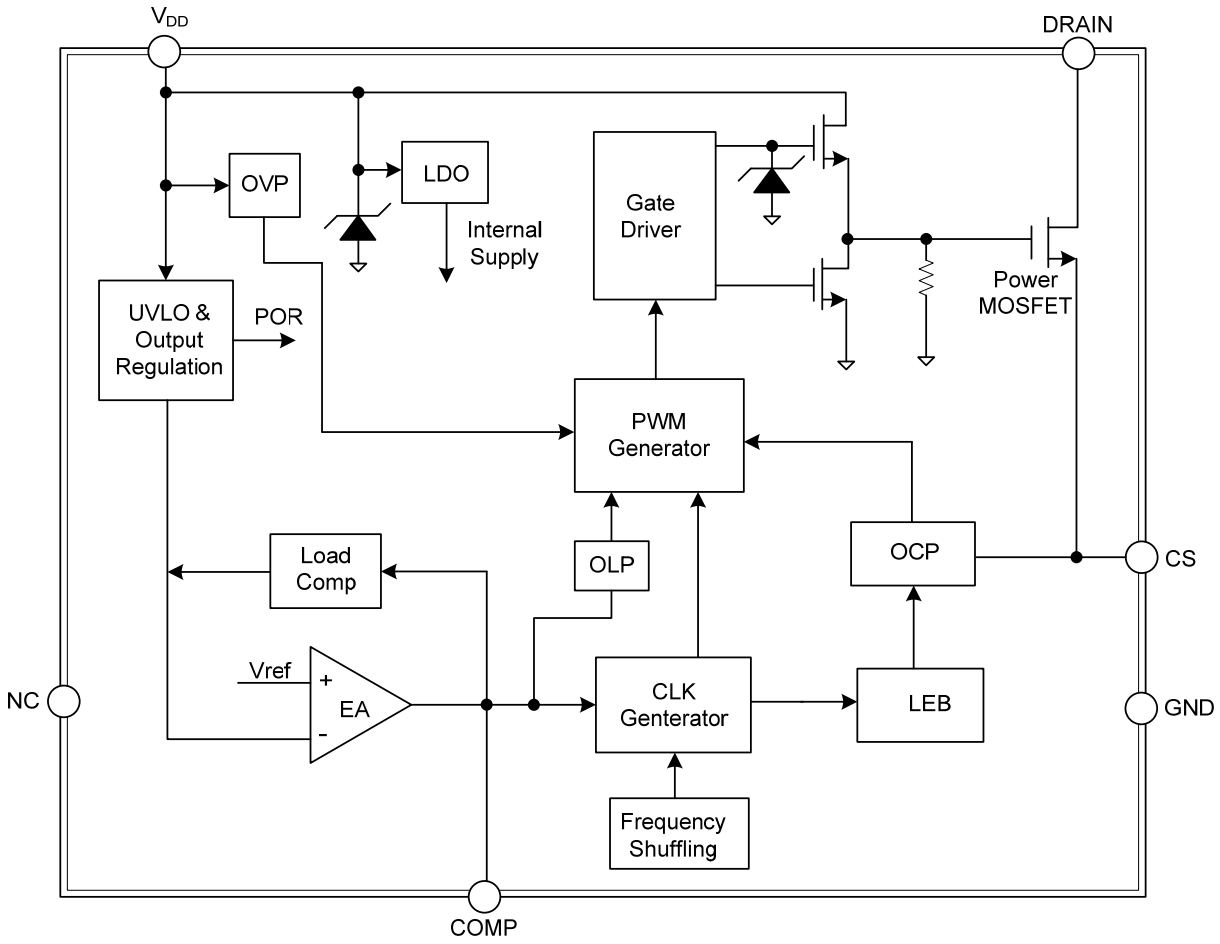
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	V_{DD}	Power supply
2	COMP	Loop compensation for CV stability
3	NC	Not connected
4	CS	Current sense input
5, 6	DRAIN	HV MOSFET Drain Pin. The Drain pin is connected to the primary lead of the transformer/ inductance.
7, 8	GND	Ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Drain Voltage (Off State)		-0.3~BVdss	V
V_{DD} Voltage		-0.3~40	V
V_{DD} Zener Clamp Continuous Current		10	mA
COMP Voltage		-0.3~7	V
CS Input Voltage		-0.3~7	V
Operating Junction Temperature	T_J	-40~150	°C
Storage Temperature	T_{STG}	-55~150	°C
Lead Temperature (Soldering, 10secs)	T_L	260	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, V_{DD}=12V, if not otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage (V_{DD}) Section						
Standby Current	$I_{DD\ ST}$	V_{DD}=13V		5	20	μA
Operation Current	$I_{DD\ OP}$	Operation Supply Current CS=0V, V_{DD}=12V		1.5	2.5	mA
VDD Under Voltage Lockout Enter	UVLO(ON)	V_{DD} Falling	7	7.8	8.6	V
VDD Under Voltage Lockout Exit	UVLO (OFF)	V_{DD} Rising	12.5	13.5	14.5	V
Over Voltage Protection Threshold	OVP	Ramp V_{DD} Until Gate Shut Down	26	27.5	29	V
In Normal Regulation, V_{DD} will be Regulated to 12V	V_{DD}	Ramp V_{DD} Until Comp Voltage Lower than 2.5V	11	12	13	V
Current Sense Input Section						
LEB Time	TLEB			200		ns
Over Current Threshold	V_{TH_OC}		910	940	970	mV
OCP Propagation Delay	$T_{D\ OC}$			110		ns
Input Impedance	$Z_{SENSE\ IN}$		50			KΩ
Frequency Section						
IC Maximum Frequency	Freq_Max		54	60	66	KHz
Frequency Shuffling Range	△f/Freq			+/-6		%
Error Amplifier Section						
DC Gain of EA	Gain			60		dB
Max. Cable Compensation Current	I_COMP_MAX	V_{DD}=12V, Comp=0V		4		μA
Power MOSFET Section						
MOSFET Drain-Source Breakdown Voltage	BV_{DSS}		600			V
On Resistance	$R_{DS(ON)}$				15	Ω

■ OPERATION DESCRIPTION

The UTC **US2351** is a cost effective PWM power switch optimized for off-line non-isolated buck applications including electrical appliance and linear regulator replacement. It operates in current mode and regulates output voltage with dedicated features. High integration can afford low cost and component count solution.

Startup Current and Start up Control

Startup current of UTC **US2351** is designed to be very low so that V_{DD} could be charged up above UVLO threshold and starts up quickly. A large value startup resistor can therefore be used to minimize the power loss in application.

Operating Current

The Operating current of UTC **US2351** is as low as 1.5mA. Good efficiency is achieved with the low operating current together with 'Muti-mode' control features.

Oscillator operation

The switching frequency of UTC **US2351** is internally fixed at 60KHZ. No external frequency setting components are required for PCB design simplification.

At light load or zero load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy. The switching frequency is internally adjusted at light load or no load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency. The minimum switching frequency is 400Hz.

Frequency shuffling for EMI improvement

The frequency shuffling (switching frequency modulation) is implemented in UTC **US2351**. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Built-in error amplifier

In UTC **US2351**, on-chip EA (error amplifier) is implemented to regulate output voltage. Through inner resistor divider, the V_{DD} voltage is detected at inverter input of EA to regulate output voltage.

Load Compensation for good CV regulation

In UTC **US2351**, load compensation is implemented to achieve good load regulation. An offset voltage is generated at inverter input of EA by an internal current flowing into the resister divider. The current is inversely proportional to the voltage across pin COMP, as a result, it is inversely proportional to the output load current, thus the output voltage can be compensated specially in zero loading condition. As the load current decreases from full-load to no-load, the offset voltage at inverter input of EA will increase.

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in UTC **US2351** current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state so that the external RC filtering on sense input is no longer needed. The PWM duty cycle is determined by the current sense input voltage and the EA output voltage.

Gate Drive

The internal power MOSFET in UTC **US2351** is driven by a dedicated gate driver for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive compromises EMI.

A good tradeoff is achieved through the built-in totem pole gate design with right output strength control.

Protection Control

Good power supply system reliability is achieved with its rich protection features including Cycle-by Cycle current limiting (OCP), Over Loading Protection, Over Voltage Protection, Output Short-Circuit Protection and Under Voltage Lockout on V_{DD} (UVLO).

■ TYPICAL APPLICATION CIRCUIT